



XC4010D, XC4013D Logic Cell Array

Product Specifications

Features

- Third Generation Field-Programmable Gate Array
 - Abundant flip-flops
 - Flexible function generators
 - No on-chip RAM
 - Dedicated high-speed carry-propagation circuit
 - Wide edge decoders (four per edge)
 - Hierarchy of interconnect lines
 - Internal 3-state bus capability
 - Eight global low-skew clock or signal distribution network
- Flexible Array Architecture
 - Programmable logic blocks and I/O blocks
 - Programmable interconnects and wide decoders
- Sub-micron CMOS Process
 - High-speed logic and Interconnect
 - Low power consumption
- Systems-Oriented Features
 - IEEE 1149.1-compatible boundary-scan logic support
 - Programmable output slew rate (2 modes)
 - Programmable input pull-up or pull-down resistors
 - 12-mA sink current per output
 - 24-mA sink current per output pair
- Configured by Loading Binary File
 - Unlimited reprogrammability
 - Six programming modes
- XACT Development System runs on '386/'486-type PC, Apollo, Sun-4, and Hewlett-Packard 700 series
 - Interfaces to popular design environments like Viewlogic, Mentor Graphics and OrCAD
 - Fully automatic partitioning, placement and routing
 - Interactive design editor for design optimization
 - 288 macros, 34 hard macros, RAM/ROM compiler

Description

The Xc4010D and XC4013D are RAM-less, lower-cost versions of the XC4010 and XC4013. They are identical to the XC4010 and XC4013 in all respects, except for the missing on-chip RAM.

The XC4010D and XC4013D are available in most of the same PLCC, PQFP, and PGA packages as their corresponding XC4000 non-D equivalents. See page 2-70 for details.

The XC4010D and XC4013D are also pin-compatible with the XC5210 (see XC5200 Data Sheet for additional information). The XC5210 provides another possible cost-reduction path for lower-performance applications that do not use the XC4000D features like wide-decoders and carry logic.

For complete electrical specifications, see pages 2-47 through 2-55.

For a detailed description of the device features, architecture and configuration methods, see pages 2-9 through 2-45.

For a detailed list of package printouts, please use the cross-reference on page 2-70.

For package physical dimensions and thermal data, see Section 4.

Table 1. The XC4000D Family of Field-Programmable Gate Arrays

| Device | XC4010/10D | XC4013/13D |
|------------------------------|------------|------------|
| Approximate Gate Count | 10,000 | 13,000 |
| CLB Matrix | 20 x 20 | 24 x 24 |
| Number of CLBs | 400 | 576 |
| Number of Flip-Flops | 1,120 | 1,536 |
| Max Decode Inputs (per side) | 60 | 72 |
| Max RAM Bits | 12,800* | 18,432* |
| Number of IOBs | 160 | 192 |

*XC4010D and XC4013D have no RAM

XC4000D Pinout Cross-Reference

| Package | XC4010 | XC4010D | XC4013 | XC4013D | XC5210 | Pinout page |
|--------------|--------|---------|--------|---------|--------|--------------------|
| 84-pin PLCC | ✓ | ✓ | | | ✓ | PC84 on page 2-62 |
| 160-pin PQFP | ✓ | ✓ | ✓ | ✓ | ✓ | PQ160 on page 2-62 |
| 191-pin PGA | ✓ | | | | | PG191 on page 2-62 |
| 208-pin PQFP | ✓ | ✓ | ✓ | ✓ | ✓ | PQ208 on page 2-62 |
| 223-pin PGA | | | ✓ | | ✓ | PG223 on page 2-64 |
| 225-pin BGA | ✓ | ✓ | ✓ | ✓ | | BG225 on page 2-64 |
| 240-pin PQFP | | | ✓ | ✓ | ✓ | PQ240 on page 2-64 |

For additional information on the XC5210, please see the **XC5200 Product Description**.

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