

••••• Combining Performance, Density, and Embedded RAM

Device Highlights

Flexible Programmable Logic

- 0.25 μm five layer metal CMOS process
- 2.5 V V_{CC} , 2.5/3.3 V drive capable I/O
- Up to 4,032 logic cells
- Up to 583,008 system gates
- Up to 347 I/O pins

Embedded Dual-Port SRAM

- Up to thirty-six 2,304-bit dual-port high performance SRAM blocks
- Up to 82,900 RAM bits
- RAM/ROM/FIFO wizard for automatic configuration
- Configurable and cascadable

Programmable I/O

- High performance enhanced I/O (EIO)—less than 3 ns T_{CO}
- Programmable slew rate control
- Programmable I/O standards:
 - LVTTTL, LVCMOS, PCI, GTL+, SSTL2, and SSTL3
 - Eight independent I/O banks
 - Three register configurations: input, output, and output enable

Advanced Clock Network

- Nine global clock networks:
 - One dedicated
 - Eight programmable
- 20 quad-net networks—five per quadrant
- 16 I/O controls—two per I/O bank
- Four phase locked loops

Embedded Computational Units

ECUs provide integrated multiply, add, and accumulate functions.

Figure 1: EclipsePlus Block Diagram

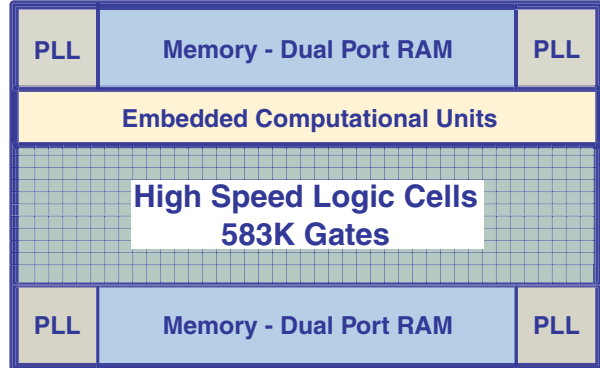


Table 1: EclipsePlus Product Family Members

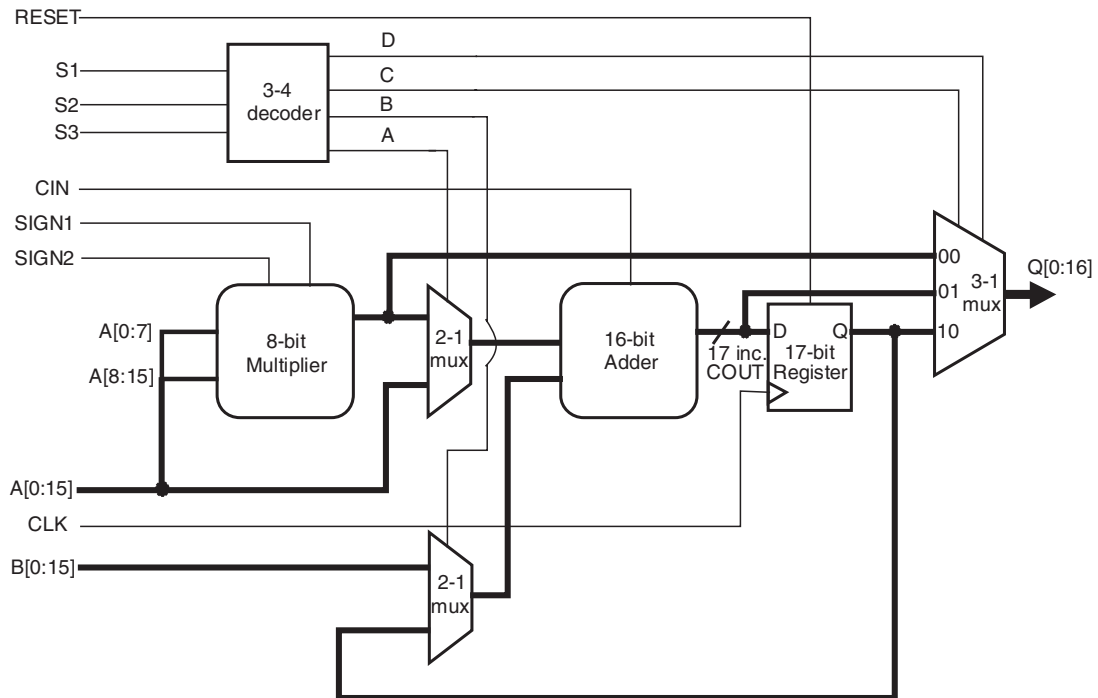
		QL7100	QL7120	QL7160	QL7180
Max Gates		292,160	373,440	558,464	662,208
Logic Array		40 x 24	48 x 32	64 x 48	72 x 56
Logic Cells		960	1,536	3,072	4,032
Max Flip-Flops		2,670	3,692	7,185	9,105
Max I/O		250	310	347	347
RAM Modules		20	24	32	36
RAM Bits		46,100	55,300	73,700	82,900
PLLs		4	4	4	4
ECUs		10	12	16	18
Packages	PQFP (0.5 mm)	208	208	-	-
	LFBGA (0.8 mm)	280	280	280	280
	PBGA (1.0 mm)	484	484	484	484
	PBGA (1.27 mm)	-	-	516	516

Embedded Computational Unit (ECU)

Traditional Programmable Logic architectures do not implement arithmetic functions efficiently or effectively—these functions require high logic cell usage while garnering only moderate performance results.

The EclipsePlus Family architecture allows for functionality above and beyond that achievable using programmable logic devices. By embedding a dynamically reconfigurable computational unit, the device can address various arithmetic functions efficiently. This approach offers greater performance than traditional programmable logic implementations. The embedded block is implemented at the transistor level as shown in **Figure 2**.

Figure 2: ECU Block Diagram



The EclipsePlus ECU blocks (**Table 2**) are placed next to the SRAM circuitry for efficient memory/instruction fetch and addressing for DSP algorithmic implementations.

Table 2: Eclipse II ECU Blocks

Device	ECUs
QL7180	18
QL7160	16
QL7120	12
QL7100	10

Up to 18 8-bit Multiply-Accumulate (MAC) functions can be implemented per cycle for a total of up to 1.8 billion MACs/s when clocked at 100 MHz. Additional MAC functions can be implemented in the programmable logic.

The modes for the ECU block are dynamically re-programmable through the programmable logic as shown in **Table 3**.

Table 3: ECU Mode Select Criteria

Instruction			Operation	ECU Performance ^a , -7 WCC ^b		
S1	S2	S3		t _{PD}	t _{SU}	t _{CO}
0	0	0	Multiply	6.57 ns max		
0	0	1	Multiply-Add	8.84 ns max		
0	1	0	Accumulate ^c		3.91 ns min.	1.16 ns max.
0	1	1	Add	3.14 ns max		
1	0	0	Multiply (registered) ^d		9.61 ns min.	1.16 ns max.
1	0	1	Multiply- Add (registered)		9.61 ns min.	1.16 ns max.
1	1	0	Multiply - Accumulate		9.61 ns min.	1.16 ns max.
1	1	1	Add (registered)		3.91 ns min.	1.16 ns max.

a. t_{PD}, t_{SU} and t_{CO} do not include routing paths in/out of the ECU block.

b. Timing numbers represent -7 Worst Case Commercial conditions.

c. Internal feedback path in ECU restricts max clk frequency to 238 MHz.

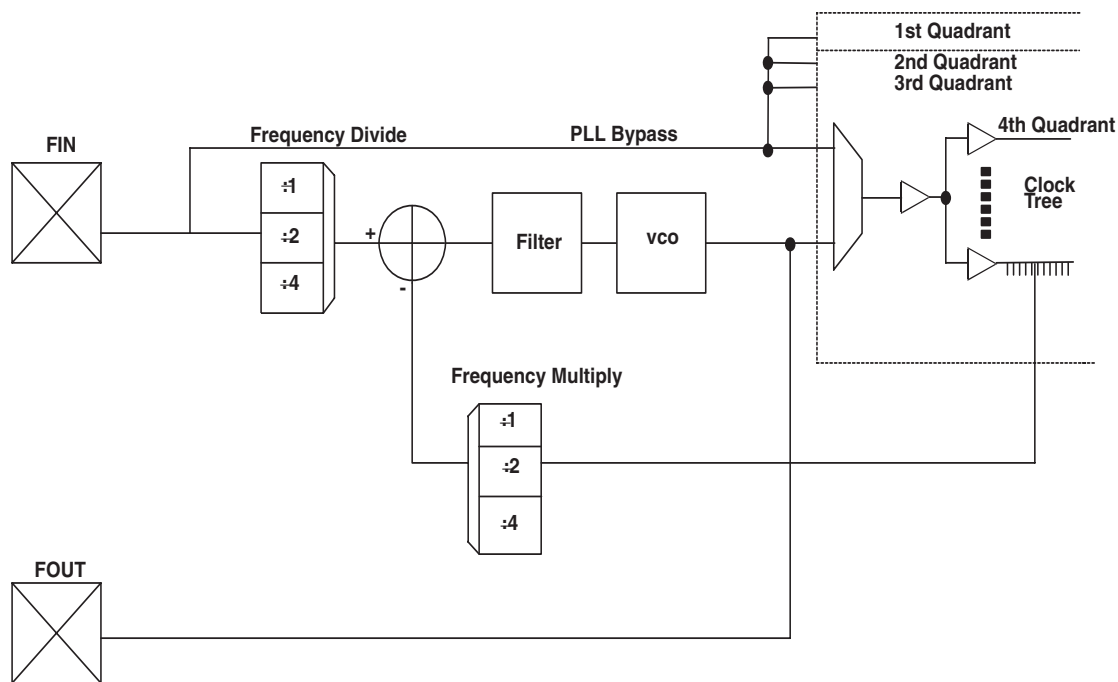
d. B [15:0] set to zero.

Phase Locked Loops (PLLs)

Instead of requiring extra components, designers simply need to instantiate one of the pre-configured models (described in this section and listed in [Table 4](#)). The QuickLogic built-in PLLs support a wider range of frequencies than many other PLLs. Also, QuickLogic PLLs can be cascaded to support different ranges of frequency multiplications or divisions, driving the device at a faster or slower rate than the incoming clock frequency. Most importantly, they achieve a very short clock-to-out time—generally less than 3 ns. This low clock-to-out time is achieved by the PLL subtracting the clock tree delay through the feedback path, effectively making the clock tree delay zero.

Figure 3 illustrates a typical QuickLogic ESP PLL.

Figure 3: PLL Block



F_{in} represents a very stable high-frequency input clock and produces an accurate signal reference. This signal can either bypass the PLL entirely, thus entering the clock tree directly, or it can pass through the PLL itself.

Within the PLL, a voltage-controlled oscillator (VCO) is added to the circuit. The external F_{in} signal and the local VCO form a control loop. The VCO is multiplied or divided down to the reference frequency, so that a phase detector (the crossed circle in [Figure 3](#)) can compare the two signals. If the phases of the external and local signals are not within the tolerance required, the phase detector sends a signal through the charge pump and loop filter ([Figure 3](#)). The charge pump generates an error voltage to bring the VCO back into alignment and the loop filter removes any high frequency noise before the error voltage enters the VCO. This new VCO signal enters the clock tree to drive the chip's circuitry.

F_{out} represents the clock signal that emerges from the output pad (the output signal PLLPAD_OUT is explained in [Table 5](#)). This clock signal is meaningful only when the PLL is configured for external use; otherwise, it remains in high Z state, as shown in the post-simulation waveform.

Most QuickLogic products contain four PLLs, one to be used in each quadrant. The PLL presented in **Figure 3** controls the clock tree in the fourth Quadrant of its ESP. As previously mentioned, QuickLogic PLLs compensate for the additional delay created by the clock tree itself by subtracting the clock tree delay through the feedback path.

For more specific information on the Phase Locked Loops, please refer to Application Note 58 at <http://www.quicklogic.com/images/appnote58.pdf>.

PLL Modes of Operation

QuickLogic PLLs have eight modes of operation, based on the input frequency and desired output frequency—**Table 4** indicates the features of each mode.

Table 4: PLL Mode Frequencies

PLL Model	Output Frequency	Input Frequency Range ^a	Output Frequency Range
PLL_HF ^b	Same as input frequency	66 MHz–150 MHz	66 MHz–150 MHz
PLL_LF	Same as input frequency	25 MHz–133 MHz	25 MHz–133 MHz
PLL_MULT2HF	2 × input frequency	50 MHz–125 MHz	100 MHz–250 MHz
PLL_MULT2LF	2 × input frequency	16 MHz–50 MHz	32 MHz–100 MHz
PLL_DIV2HF	1/2 × input frequency	100 MHz–250 MHz	50 MHz–125 MHz
PLL_DIV2LF	1/2 × input frequency	50 MHz–100 MHz	25 MHz–50 MHz
PLL_MULT4	4 × input frequency	16 MHz–40 MHz	64 MHz–160 MHz
PLL_DIV4	1/4 × input frequency	100 MHz–300 MHz	25 MHz–75 MHz

a. The input frequency can range from 12.5 MHz to 500 MHz, while output frequency ranges from 25 MHz to 250 MHz. When you add PLLs to your top-level design, be sure that the PLL mode matches your desired input and output frequencies.

b. HF stands for high frequency and LF stands for low frequency.

PLL Signals

Table 5 summarizes the key signals in QuickLogic's PLLs.

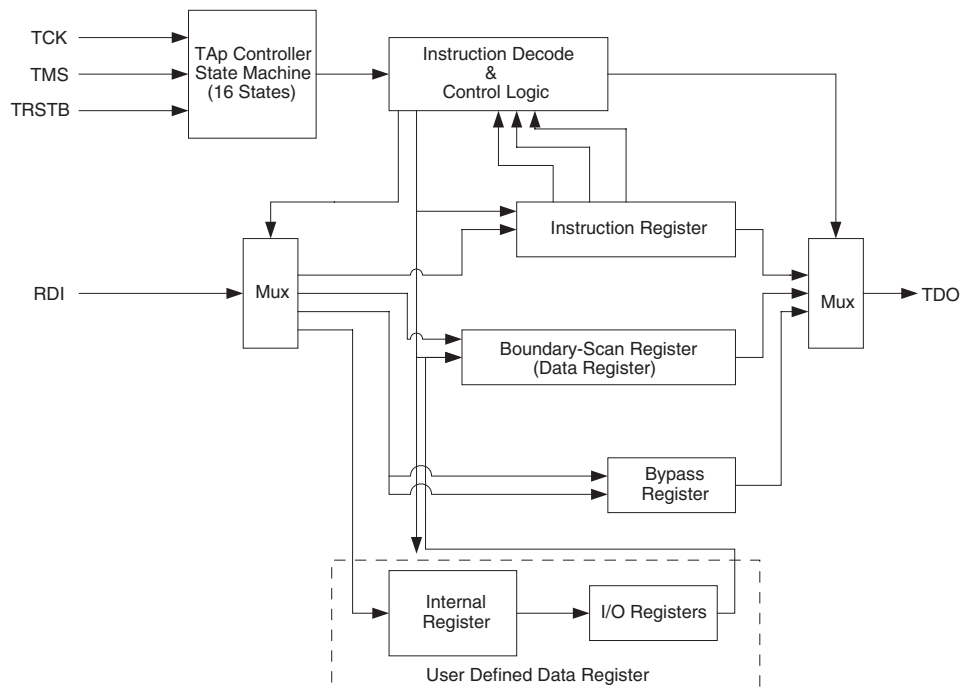
Table 5: PLL Signals

Signal Name	Description
PLLCLK_IN ^a	Input clock signal
PLLRST	Active High Reset If PLLRST is asserted, then CLKNET_OUT and PLLPAD_OUT are reset to 0. This signal must be asserted and then released in order for the LOCK_DETECT to work.
ONn_OFFCHIP	PLL output This signal selects whether the PLL will drive the internal clock network or be used off-chip. This is a static signal, not a dynamic signal. Tied to GND = outgoing signal drives internal gates. Tied to VCC = outgoing signal used off-chip.
CLKNET_OUT	Out to internal gates This signal bypasses the PLL logic before driving the internal gates. Note that this signal cannot be used in the same quadrant where the PLL signal is used (PLLCLK_OUT).
PLLCLK_OUT	Out from PLL to internal gates This signal can drive the internal gates after going through the PLL. For this to work, ONn_OFFCHIP must be tied to GND.
PLLPAD_OUT	Out to off-chip This outgoing signal is used off-chip. For this to work, ONn_OFFCHIP signal must be tied to VCC.
LOCK_DETECT	Active High Lock detection signal NOTE: For simulation purposes, this signal gets asserted after 10 clock cycles. However, it can take a maximum of 200 clock cycles to sync with the input clock upon release of the RESET signal.

a. Because PLLCLK_IN and PLLRST signals have INPAD, and PLLPAD_OUT has OUTPAD, you do not have to add additional pads to your design.

Joint Test Access Group (JTAG)

Figure 4: JTAG Block Diagram



Microprocessors and Application Specific Integrated Circuits (ASICs) pose many design challenges, one problem being the accessibility of test points. The Joint Test Access Group (JTAG) formed in response to this challenge, resulting in IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture.

The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR), which allow users to run three required tests along with several user-defined tests.

JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for fuller verification of higher level system elements.

The 1149.1 standard requires the following three tests:

- **Extest Instruction.** The Extest instruction performs a PCB interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP's Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (via the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction.** This instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed via a data scan operation, allowing users to sample the functional data entering and leaving the device.
- **Bypass Instruction.** The Bypass instruction allows data to skip a device's boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register is connected between the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

Electrical Specifications

AC Characteristics*

*(at $V_{CC} = 2.5\text{ V}$, $T_A = 25^\circ\text{ C}$, Typical Corner, Speed Grade = -7 (K = 1.00))

The AC Specifications are provided from **Table 6** to **Table 14**. Logic Cell diagrams and waveforms are provided from **Figure 5** to **Figure 18**.

Figure 5: EclipsePlus Logic Cell

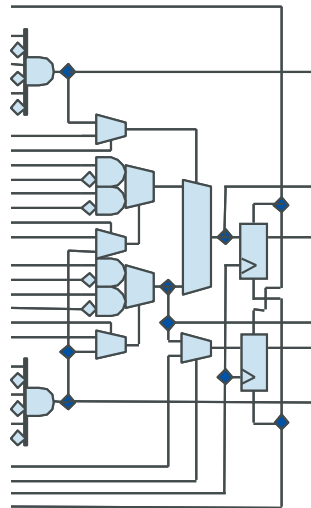


Table 6: Logic Cells

Symbol	Parameter	Value (ns)	
		Min.	Max.
t_{PD}	Combinatorial Delay of the longest path: time taken by the combinatorial circuit to output	0.205	1.01
t_{SU}	Setup time: time the synchronous input of the flip flop must be stable before the active clock edge	0.231	-
t_{HL}	Hold time: time the synchronous input of the flip flop must be stable after the active clock edge	0	-
t_{CO}	Clock to out delay: the amount of time taken by the flip flop to output after the active clock edge.	-	0.427
t_{CWHI}	Clock High Time: required minimum time the clock stays high	0.46	-
t_{CWL0}	Clock Low Time: required minimum time that the clock stays low	0.46	-
t_{SET}	Set Delay: time between when the flip flop is "set" (high) and when the output is consequently "set" (high)	-	0.585

Table 6: Logic Cells (Continued)

Symbol	Parameter	Value (ns)	
		Min.	Max.
t_{RESET}	Reset Delay: time between when the flip flop is "reset" (low) and when the output is consequently "reset" (low)	-	0.658
t_{SW}	Set Width: time that the SET signal remains high/low	0.3	-
t_{RW}	Reset Width: time that the RESET signal remains high/low	0.3	-

Figure 6: Logic Cell Flip-Flop

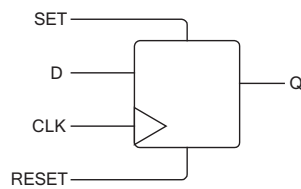


Figure 7: Logic Cell Flip-Flop Timings—First Waveform

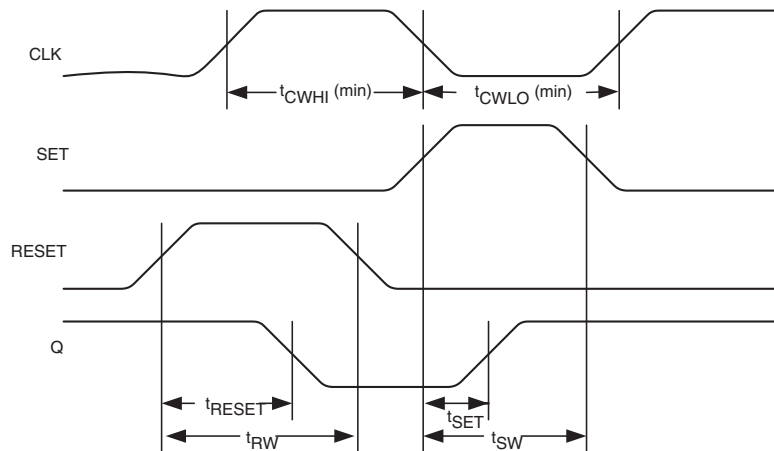


Figure 8: Logic Cell Flip-Flop Timings—Second Waveform

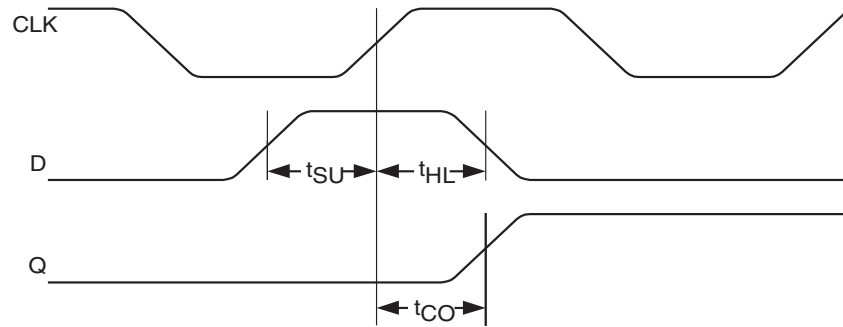


Figure 9: EclipsePlus Global Clock Structure

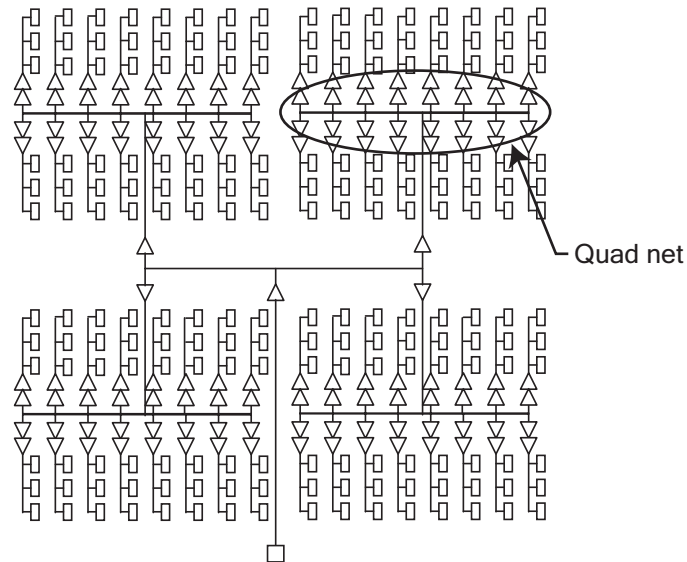


Table 7: Eclipse Global Clock Tree Delays

Clock Segment	Parameter	Value (ns)	
		Max. Rise	Max. Fall
t_{PGCK}	Global clock pin delay to quad net	0.990	1.386
t_{BGCK}	Global clock buffer delay (quad net to flip flop)	0.534	1.865

Figure 10: Global Clock Structure Schematic

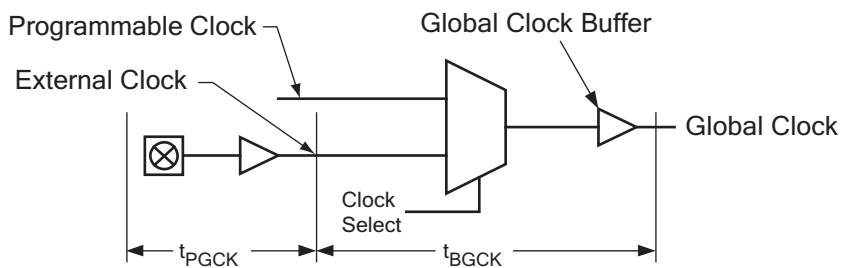


Figure 11: RAM Module

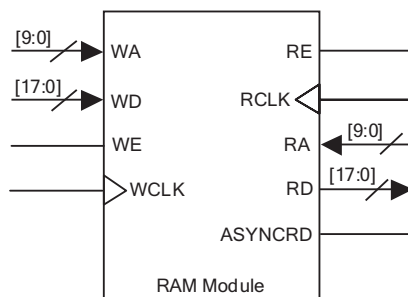


Table 8: RAM Cell Synchronous Write Timing

Symbol	Parameter	Value (ns)	
		Min.	Max.
t_{SWA}	WA setup time to WCLK: time the WRITE ADDRESS must be stable before the active edge of the WRITE CLOCK	0.675 ns	-
t_{HWA}	WA hold time to WCLK: time the WRITE ADDRESS must be stable after the active edge of the WRITE CLOCK	0 ns	-
t_{SWD}	WD setup time to WCLK: time the WRITE DATA must be stable before the active edge of the WRITE CLOCK	0.654 ns	-
t_{HWD}	WD hold time to WCLK: time the WRITE DATA must be stable after the active edge of the WRITE CLOCK	0 ns	-
t_{SWE}	WE setup time to WCLK: time the WRITE ENABLE must be stable before the active edge of the WRITE CLOCK	0.276 ns	-
t_{HWE}	WE hold time to WCLK: time the WRITE ENABLE must be stable after the active edge of the WRITE CLOCK	0 ns	-
t_{WCRD}	WCLK to RD (WA = RA): time between the active WRITE CLOCK edge and the time when the data is available at RD	-	2.796 ns

Figure 12: RAM Cell Synchronous Write Timing

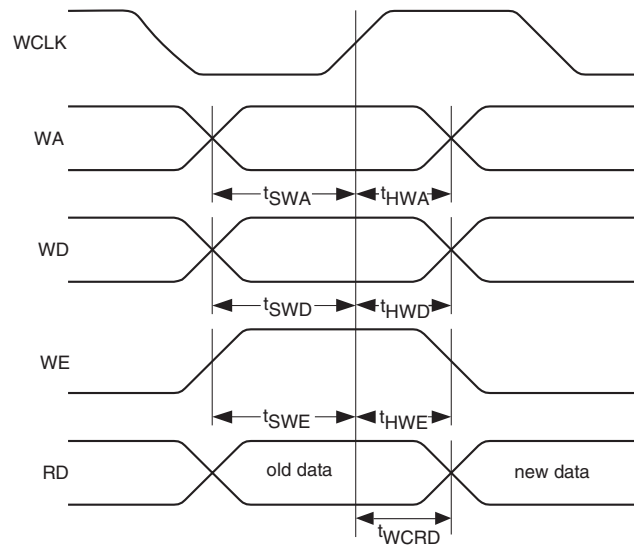


Table 9: RAM Cell Synchronous & Asynchronous Read Timing

Symbol	Parameter	Value (ns)	
		Min.	Max.
RAM Cell Synchronous Read Timing			
t_{SRA}	RA setup time to RCLK: time the READ ADDRESS must be stable before the active edge of the READ CLOCK	0.686 ns	-
t_{HRA}	RA hold time to RCLK: time the READ ADDRESS must be stable after the active edge of the READ CLOCK	0 ns	-
t_{SRE}	RE setup time to WCLK: time the READ ENABLE must be stable before the active edge of the READ CLOCK	0.243 ns	-
t_{HRE}	RE hold time to WCLK: time the READ ENABLE must be stable after the active edge of the READ CLOCK	0 ns	-
t_{RCRD}	RCLK to RD: time between the active READ CLOCK edge and the time when the data is available at RD	-	2.225 ns
RAM Cell Asynchronous Read Timing			
t_{PDRD}	RA to RD: time between when the READ ADDRESS is input and when the DATA is output	-	2.405 ns

Figure 13: RAM Cell Synchronous & Asynchronous Read Timing

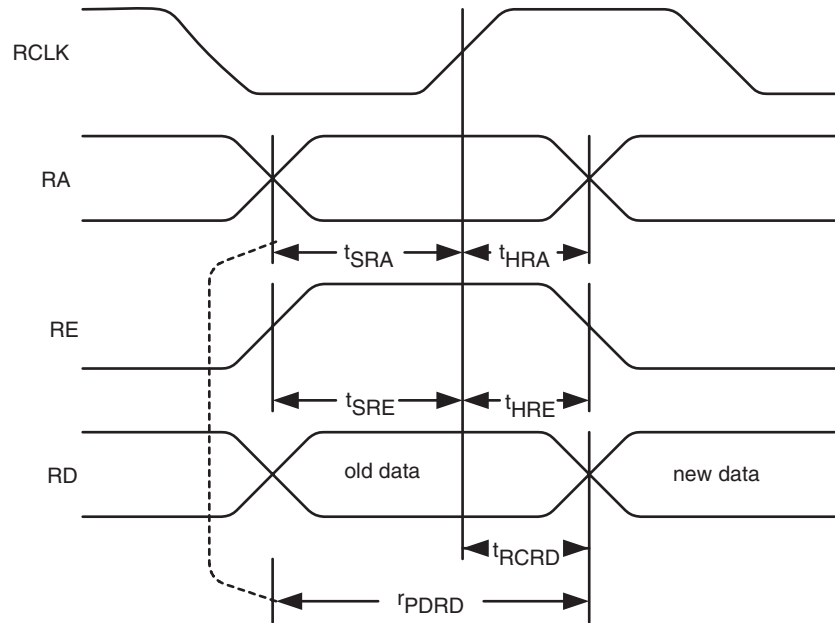


Figure 14: EclipsePlus Cell I/O

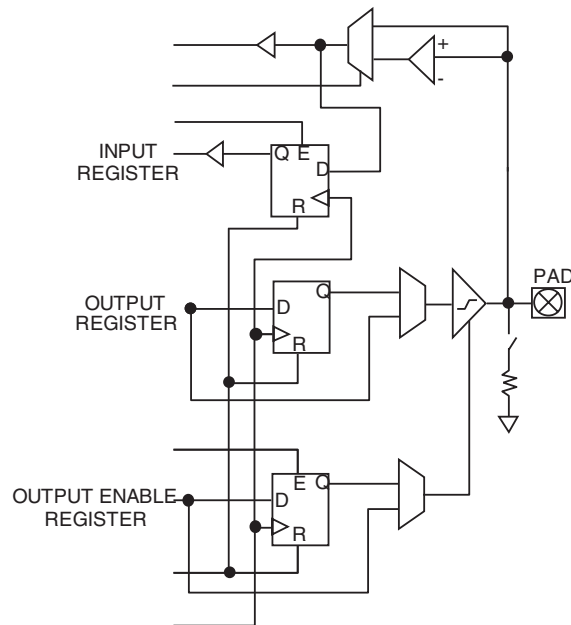


Figure 15: EclipsePlus Input Register Cell

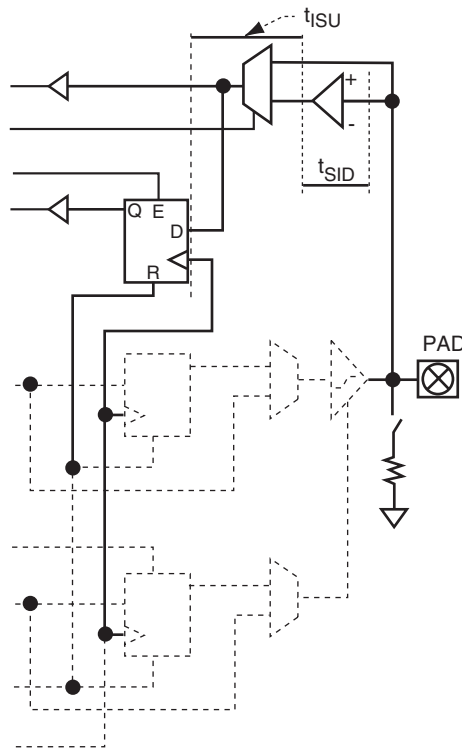


Table 10: Input Register Cell

Symbol	Parameter	Value (ns)	
		Min.	Max.
t_{ISU}	Input register setup time: the time the synchronous input of the pin must be stable before the active clock edge	3.308 ns	3.526 ns
t_{IHL}	Input register hold time: the time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	-
t_{ICO}	Input register clock-to-out: the time taken by the flip-flop to output after the active clock edge	-	0.494 ns
t_{IRST}	Input register reset delay: the time between when the flip-flop is "reset" (low) and when the output is consequently "reset" (low)	-	0.464 ns
t_{IESU}	Input register clock enable setup time: the time "enable" must be stable before the active clock edge	0.830 ns	0.987 ns
t_{IEH}	Input register clock enable hold time: the time "enable" must be stable after the active clock edge	0 ns	-

Table 11: Standard Input Delays

Symbol	Parameter	Value (ns)	
		Min.	Max.
t_{SID} (LVTTTL)	LVTTTL input delay: Low Voltage TTL for 3.3 V applications	-	0.34
t_{SID} (LVCMOS2)	LVCMOS2 input delay: Low Voltage CMOS for 2.5 V and lower applications	-	0.42
t_{SID} (GTL+)	GTL+ input delay: Gunning Transceiver Logic	-	0.68
t_{SID} (SSTL3)	SSTL3 input delay: Stub Series Terminated Logic for 3.3 V	-	0.55
t_{SID} (SSTL2)	SSTL2 input delay: Stub Series Terminated Logic for 2.5 V	-	0.61

Figure 16: EclipsePlus Input Register Cell Timing

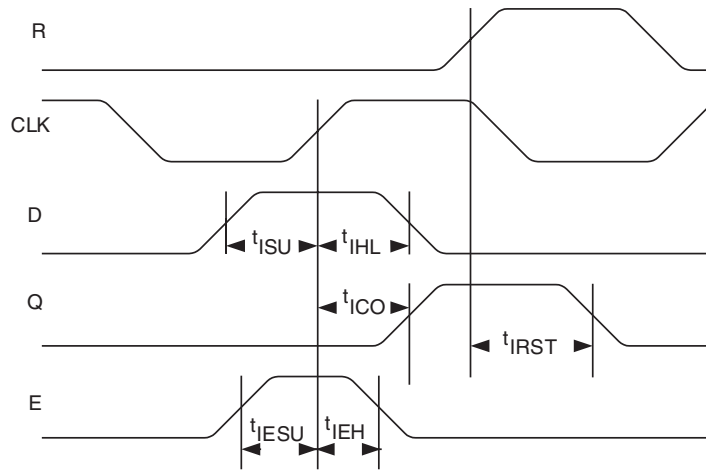


Figure 17: EclipsePlus Output Register Cell

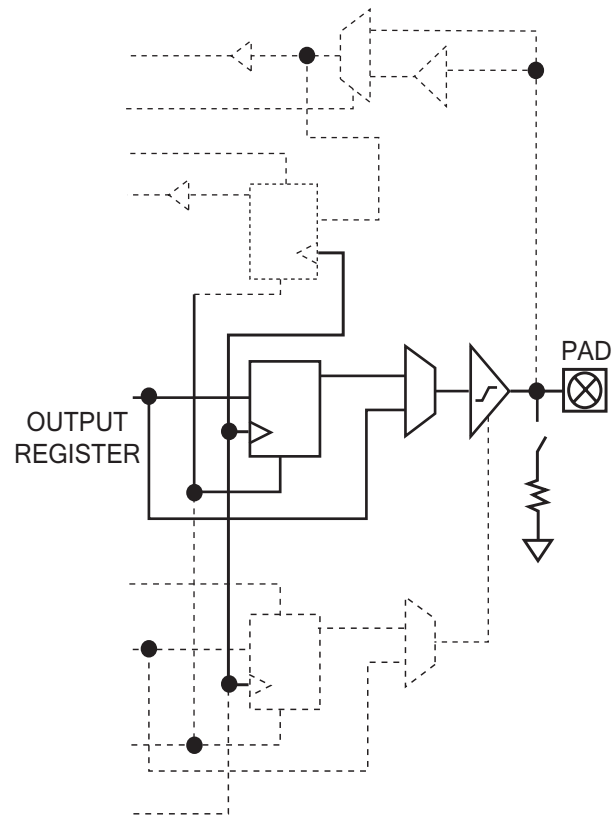


Table 12: EclipsePlus Output Register Cell

Symbol	Parameter	Value	
		Min.	Max.
Output Register Cell Only			
t_{OUTLH}	Output Delay low to high (90% of H)	-	0.40 ns
t_{OUTHl}	Output Delay high to low (10% of L)	-	0.55 ns
t_{PZH}	Output Delay tri-state to high (90% of H)	-	2.94 ns
t_{PZL}	Output Delay tri-state to low (10% of L)	-	2.34 ns
t_{PHZ}	Output Delay high to tri-State	-	3.07 ns
t_{PLZ}	Output Delay low to tri-State	-	2.53 ns
t_{COP}	Clock-to-out delay (does not include clock tree delays)	-	3.15 ns (fast slew) 10.2 ns (slow slew)

Figure 18: EclipsePlus Output Register Cell Timing

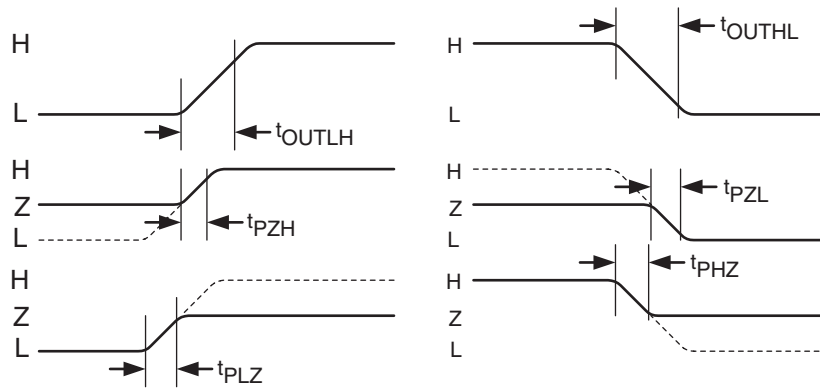


Table 13: Output Slew Rates @ $V_{CCIO} = 3.3\text{ V}$

	Fast Slew	Slow Slew
Rising Edge	2.8 V/ns	1.0 V/ns
Falling Edge	2.86 V/ns	1.0 V/ns

Table 14: Output Slew Rates @ $V_{CCIO} = 2.5\text{ V}$

	Fast Slew	Slow Slew
Rising Edge	1.7 V/ns	0.6 V/ns
Falling Edge	1.9 V/ns	0.6 V/ns

NOTE: For tips to minimize ground bounce, refer to Application Note 66 at <http://www.quicklogic.com/images/appnote66.pdf>.

DC Characteristics

The DC Specifications are provided in **Table 15** through **Table 20**.

Table 15: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
V _{CC} Voltage	-0.5 V to 3.6 V	DC Input Current	±20 mA
V _{CCIO} Voltage	-0.5 V to 4.6 V	ESD Pad Protection	±2000 V
INREF Voltage	2.7 V	Leaded Package Storage Temperature	-65° C to + 150° C
Input Voltage ^a	-0.5 V to V _{CCIO} +0.5 V	Laminate Package (BGA) Storage Temperature	-55° C to + 125° C
Latch-up Immunity	±100 mA		

a. All dedicated inputs including the CLK, DEDCLK, PLLIN, PLLRST, and IOCTRL pins, are clamped to the V_{CC} rail, not the V_{CCIO}. Therefore, these pins can only be driven up to V_{CC} + 0.3 V. These input pins are LVCMOS2 compliant only (2.5 V).

Table 16: Recommended Operating Range

Symbol	Parameter	Military		Industrial		Commercial		Unit	
		Min.	Max.	Min.	Max.	Min.	Max.		
VCC	Supply Voltage	2.3	2.7	2.3	2.7	2.3	2.7	V	
VCCIO	I/O Input Tolerance Voltage	2.3	3.6	2.3	3.6	2.3	3.6	V	
TJ	Ambient Temperature	-55	-	-40	85	0	70	°C	
TC	Case Temperature	-	125	-	-	-	-	°C	
K	Delay Factor	-4 Speed Grade	0.42	2.3	0.43	2.16	0.47	2.11	n/a
		-5 Speed Grade	0.42	1.92	0.43	1.80	0.46	1.76	n/a
		-6 Speed Grade	0.42	1.35	0.43	1.26	0.46	1.23	n/a
		-7 Speed Grade	0.42	1.27	0.43	1.19	0.46	1.16	n/a

Table 17: DC Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Units
I_I	I or I/O Input Leakage Current	$V_I = V_{CCIO}$ or GND	-10	10	μA
I_{OZ}	3-State Output Leakage Current	$V_I = V_{CCIO}$ or GND	-10	10	μA
C_I	Input Capacitance ^a	-	-	8	pF
I_{OS}	Output Short Circuit Current ^b	$V_o = \text{GND}$ $V_o = V_{CC}$	-15 40	-180 210	mA mA
I_{CC}	D.C. Supply Current ^c	$V_I, V_o = V_{CCIO}$ or GND	0.50 (typ.)	2	mA
I_{CCIO}	D.C. Supply Current on V_{CCIO}	-	0	2	mA
$I_{CCIO}(\text{DIF})$	D.C. Supply Current on V_{CCIO} for Differential I/O	-	-	-	mA
I_{REF}	D.C. Supply Current on INREF	-	-10	10	μA
I_{PD}	Pad Pull-down (programmable)	$V_{CCIO} = 3.6 \text{ V}$	-	150	μA

a. Capacitance is sample tested only. Clock pins are 12 pF maximum.

b. Only one output at a time. Duration should not exceed 30 seconds.

c. For -4/-5/-6/-7 commercial grade devices only. See [Table 18](#) for more details on I_{CC} characteristics.

Table 18: I_{CC} Characteristics

Characteristic	Condition	Temperature		
		Commercial	Industrial	Military
I_{CC}	$V_{CCPLL} = \text{GND}$	2 mA (max)	3 mA (max)	5 mA (max)
	$V_{CCPLL} = V_{CC}$	3.25 mA (max)	5 mA (max)	10 mA (max)

NOTE: If PLLs are not used, the V_{CCPLL} and PLLRST pins may be grounded to the lower I_{CC} for the device.

Table 19: DC Input and Output Levels^a

	INREF		V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MAX}	V_{MIN}	mA	mA
LVTTL	n/a	n/a	-0.3	0.8	2.0	$V_{CCIO} + 0.3$	0.4	2.4	2.0	-2.0
LVCOS2	n/a	n/a	-0.3	0.7	1.7	$V_{CCIO} + 0.3$	0.7	1.7	2.0	-2.0
GTL+	0.88	1.12	-0.3	INREF - 0.2	INREF + 0.2	$V_{CCIO} + 0.3$	0.6	n/a	40	n/a
PCI	n/a	n/a	-0.3	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.5$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5
SSTL2	1.15	1.35	-0.3	INREF - 0.18	INREF + 0.18	$V_{CCIO} + 0.3$	0.74	1.76	7.6	-7.6
SSTL3	1.3	1.7	-0.3	INREF - 0.2	INREF + 0.2	$V_{CCIO} + 0.3$	1.10	1.90	8	-8

a. The data provided in [Table 19](#) are JEDEC and PCI Specifications. QuickLogic devices either meet or exceed these requirements. For data specific to QuickLogic I/Os, see [Table 10](#) through [Table 20](#) and [Figure 14](#) through [Figure 20](#).

NOTE: All CLK and IOCTRL pins are clamped to the V_{CC} rail, not the V_{CCIO} . Therefore, these pins can only be driven up to $V_{CC} + 0.3 \text{ V}$.

NOTE: All dedicated inputs including the CLK, DEDCLK, PLLIN, PLLRST, and IOCTRL pins, are clamped to the V_{CC} rail, not the V_{CCIO} . Therefore, these pins can only be driven up to $V_{CC} + 0.3 \text{ V}$. These input pins are LVCOS2 compliant only (2.5 V).

I/O Characteristics

Figure 19: IOL vs. VOL

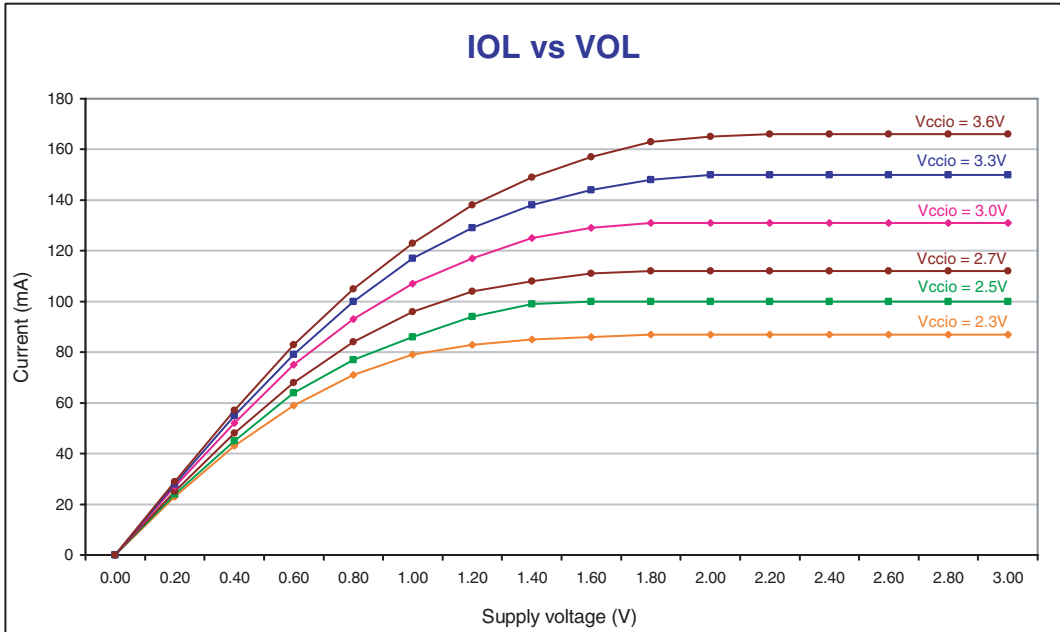


Figure 20: IOH vs. VOH

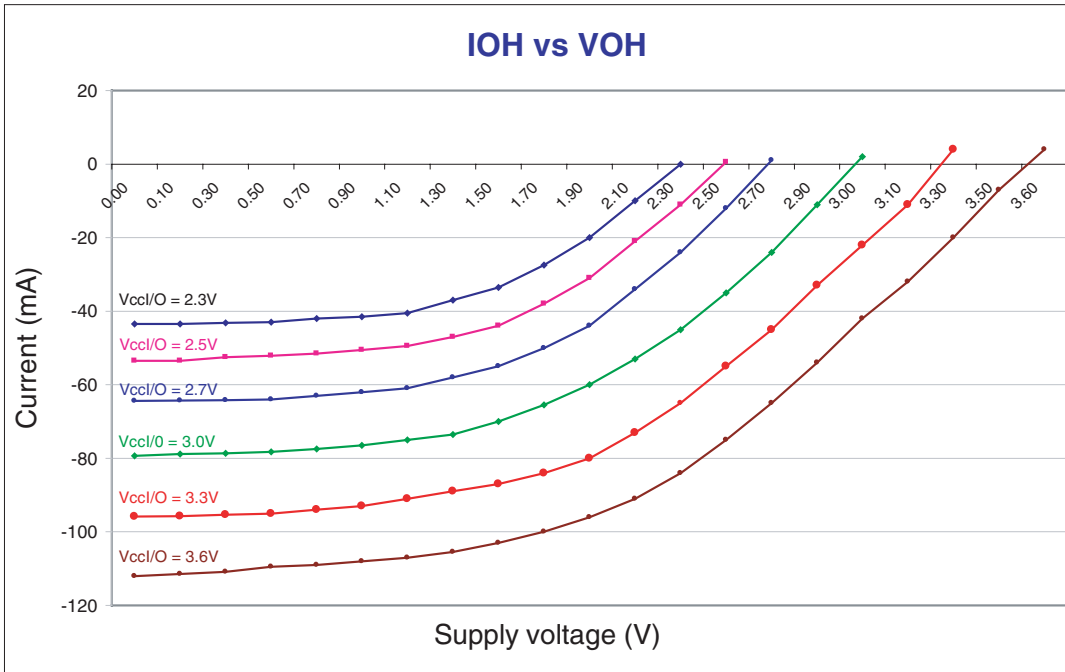


Table 20: Max I/O per Device /Package Combination

Device	208 PQFP	280 LFBGA	484 PBGA	516 PBGA
QL7100	99	163	250	-
QL7120	99	163	310	-
QL7160	-	163	327	347
QL7180	-	163	327	347

Package Thermal Characteristics

Thermal Resistance Equations:

$$\theta_{JC} = (T_J - T_C) / P$$

$$\theta_{JA} = (T_J - T_A) / P$$

$$P_{MAX} = (T_{JMAX} - T_{AMAX}) / \theta_{JA}$$

Parameter Description:

θ_{JC} : Junction-to-case thermal resistance

θ_{JA} : Junction-to-ambient thermal resistance

T_J : Junction temperature

T_A : Ambient temperature

P: Power dissipated by the device while operating

P_{MAX} : The maximum power dissipation for the device

T_{JMAX} : Maximum junction temperature

T_{AMAX} : Maximum ambient temperature

NOTE: Maximum junction temperature (T_{JMAX}) is 150°C. To calculate the maximum power dissipation for a device package look up θ_{JA} from **Table 21**, pick an appropriate T_{AMAX} and use:

$$P_{MAX} = (150^\circ\text{C} - T_{AMAX}) / \theta_{JA}$$

Table 21: Package Thermal Characteristics

Package Description		θ_{JA} (°C/W) @ various flow rates (m/sec)				θ_{JC} (°C/W)
Pin Count	Package Type	0	0.5	1	2	
516	PBGA	20.0	19.0	17.5	16.0	7.0
484	PBGA	28.0	26.0	25.0	23.0	9.0
280	LFBGA	18.5	17.0	15.5	14.0	7.0
208	PQFP	26.0	24.5	23.0	22.0	11.0

Kv and Kt Graphs

Figure 21: Voltage Factor vs. Supply Voltage

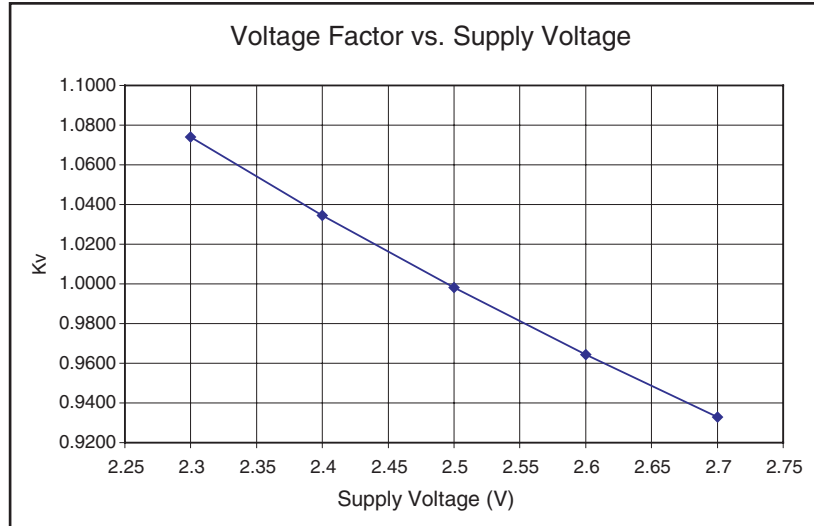
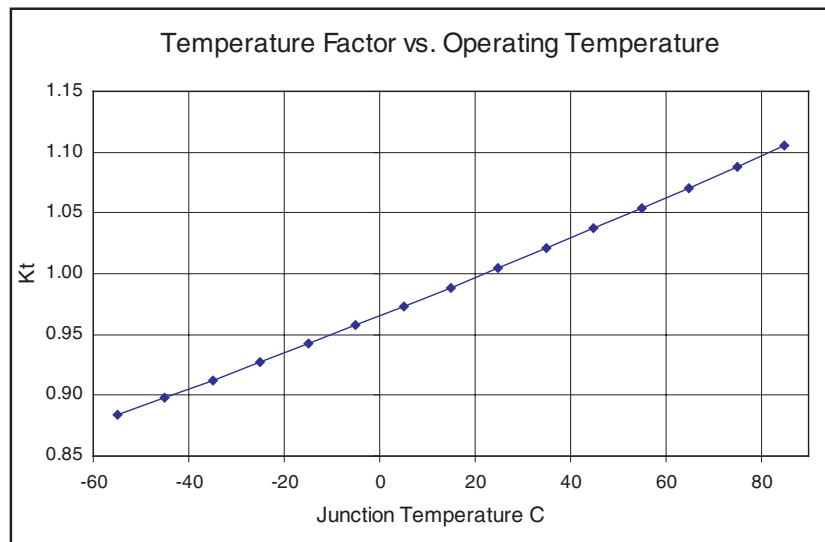


Figure 22: Temperature Factor vs. Operating Temperature



Power vs. Operating Frequency

The basic power equation which best models power consumption is given below:

$$P_{\text{TOTAL}} = 0.350 + f[0.0031 \eta_{\text{LC}} + 0.0948 \eta_{\text{CKBF}} + 0.01 \eta_{\text{CLBF}} + 0.0263 \eta_{\text{CKLD}} + 0.543 \eta_{\text{RAM}} + 0.20 \eta_{\text{PLL}} + 0.0035 \eta_{\text{INP}} + 0.0257 \eta_{\text{OUTP}}] \text{ (mW)}$$

Where:

η_{LC} is the total number of logic cells in the design

η_{CKBF} = # of clock buffers

η_{CLBF} = # of column clock buffers

η_{CKLD} = # of loads connected to the column clock buffers

η_{RAM} = # of RAM blocks

η_{PLL} = # of PLLs

η_{INP} is the number of input pins

η_{OUTP} is the number of output pins

Figure 23 exhibits the power consumption in an EclipsePlus device. The chip was filled with (300) 8-bit counters—approximately 76% logic cell utilization.

Figure 23: Power Consumption

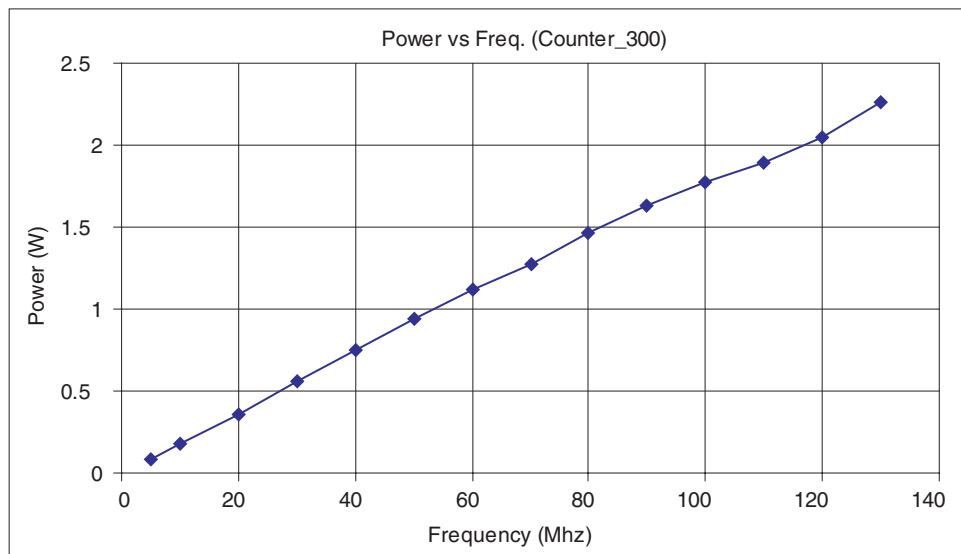
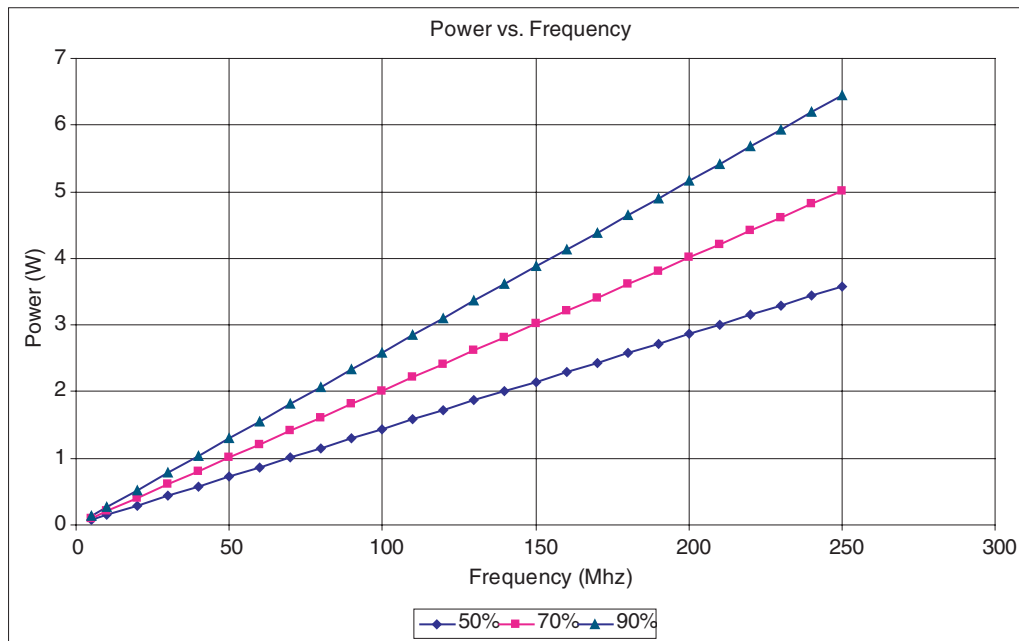


Figure 24 illustrates the theoretical worst-case scenarios for 50%, 70%, and 90% utilizations of the QL7160/QL7180-516 package. The resources of the device are divided exactly in half; meaning, for 50% utilization, exactly 50% of the I/Os, Logic Cells, RAM blocks, clock network, etc. are utilized. These situations may never occur in a real design, but they do provide a very rough quantitative measure of power consumption when talking in terms of 50% or 70% utilization of an EclipsePlus device.

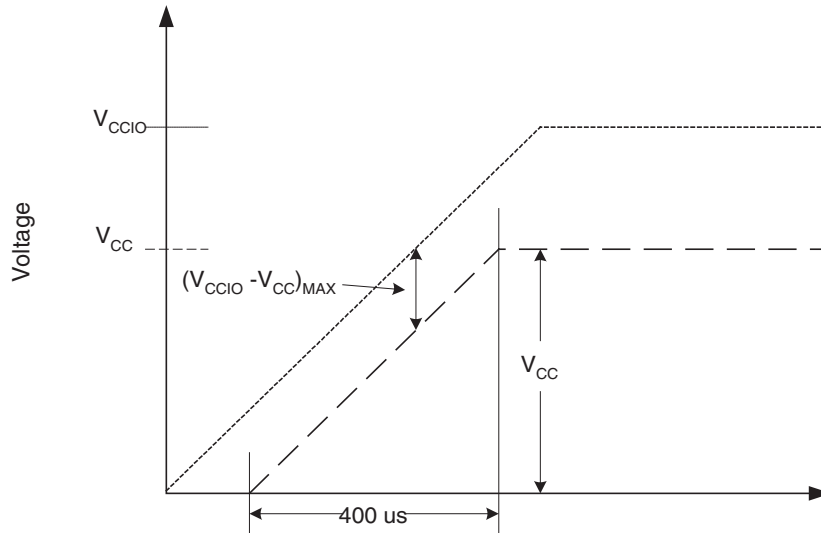
Figure 24: Power vs. Frequency (Absolute 50%, 70%, and 90% of the Available Resources on Chip)



NOTE: To learn more about power consumption, see QuickLogic Application Note 60 at <http://www.quicklogic.com/images/appnote60.pdf>.

Power-Up Sequencing

Figure 25: Power-Up Requirements



When powering up a device, the V_{CC}/V_{CCIO} rails must take 400 μs or longer to reach the maximum value (refer to **Figure 25**).

NOTE: Ramping V_{CC}/V_{CCIO} to the maximum voltage faster than 400 μs can cause the device to behave improperly.

For users with a limited power budget, keep $(V_{CCIO} - V_{CC})_{MAX} \leq 500$ mV when ramping up the power supply.

Pin Descriptions

Table 22: JTAG Pin Descriptions

Pin	Function	Description
TDI/RSI	Test Data In for JTAG/RAM init. Serial Data In	Hold HIGH during normal operation. Connects to serial PROM data in for RAM initialization. Connect to V_{CC} if unused
TRSTB/RRO	Active low Reset for JTAG/RAM init. reset out	Hold LOW during normal operation. Connects to serial PROM reset for RAM initialization. Connect to GND if unused
TMS	Test Mode Select for JTAG	Hold HIGH during normal operation. Connect to V_{CC} if not used for JTAG
TCK	Test Clock for JTAG	Hold HIGH or LOW during normal operation. Connect to V_{CC} or ground if not used for JTAG
TDO/RCO	Test data out for JTAG/RAM init. clock out	Connect to serial PROM clock for RAM initialization. Must be left unconnected if not used for JTAG or RAM initialization

NOTE: All JTAG inputs are clamped to the V_{CC} rail, not the V_{CCIO} . Therefore, these pins can only be driven up to $V_{CC} + 0.3$ V. These input pins are LVCMOS2 compliant only (2.5 V). All JTAG outputs are driven by the V_{CC} rail, not V_{CCIO} . Therefore, these output pins can only drive up to $V_{CC} + 0.3$ V. These output pins are LVCMOS2 compliant only (2.5 V).

Figure 26: I/O Banks with Relevant Pins

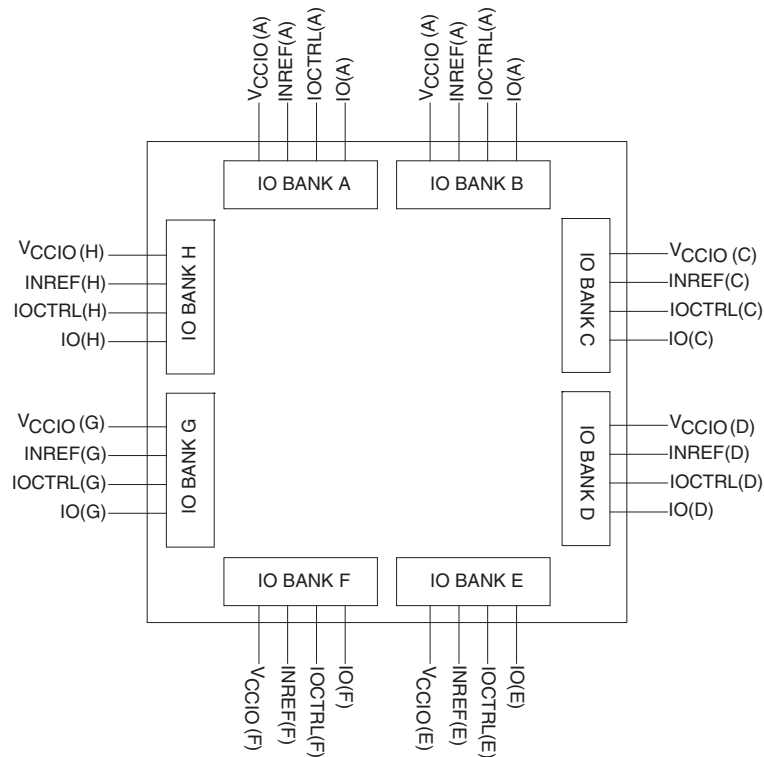


Table 23: Dedicated Pin Descriptions

Pin	Direction	Function	Description
CLK ^a	I	Global clock network driver	Low skew global clock. This pin provides access to a dedicated, distributed network capable of driving the CLOCK, SET, RESET, F1, and A2 inputs to the Logic Cell, READ, and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, CLOCK of the ECUs, and Output Enables of the I/Os.
I/O(A)	I/O	Input/Output pin	The I/O pin is a bi-directional pin, configurable to either an input-only, output-only, or bi-directional pin. The A inside the parenthesis means that the I/O is located in Bank A. If an I/O is not used, SpDE (QuickWorks Tool) provides the option of tying that pin to GND, V _{CC} , or TriState during programming.
V _{CC}	I	Power supply pin	Connect to 2.5 V supply
V _{CCIO(A)}	I	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V device or a 2.5 V device. The A inside the parenthesis means that V _{CCIO} is located in BANK A. Every I/O pin in Bank A will be tolerant of V _{CCIO} input signals and will output V _{CCIO} level signals. This pin must be connected to either 3.3 V or V _{CC} .
V _{CCPLL} ^b	I	Phase locked loop power supply pin	Connect to 2.5 V supply. VCCPLL should be connected to 2.5 V supply if the PLLs are used. If the PLLs are not used, V _{CCPLL} can be connected to 2.5 V supply or GND. See Table 18 for I ^{CC} differences when V _{CCPLL} is connected to 2.5 V or GND.
GND	I	Ground pin	Connect to ground
PLLIN ^a	I	PLL clock input	Clock input for PLL
DEDCLK ^a	I	Dedicated clock pin	Low skew global clock. This pin provides access to a dedicated, distributed clock network capable of driving the CLOCK inputs of all sequential elements of the device (e.g. RAM, Flip Flops).
GNDPLL	I	Ground pin for PLL	Connect to GND
INREF(A)	I	Differential reference voltage	The INREF is the reference voltage pin for GTL+, SSTL2, and STTL3 standards. Follow the recommendations provided in Table 21 for the appropriate standard. The A inside the parenthesis means that INREF is located in BANK A. This pin should be tied to GND if not needed.
PLLOUT	O	PLL output pin	Dedicated PLL output pin. Otherwise may be left unconnected
PLL _{RST} ^a	I	Reset input pin for PLL	Reset input for PLL. If PLLs are not used, PLL _{RST} should be connected to the same voltage as V _{CCPLL} (e.g., V _{CC} or GND).
IOCTRL(A) ^a	I	High drive input	This pin provides fast RESET, SET, CLOCK, and ENABLE access to the I/O cell flip-flops, providing fast clock-to-out and fast I/O response times. This pin can also double as a high-drive pin to the internal logic cells. The A inside the parenthesis means that IOCTRL is located in Bank A. This pin should be tied to GND or V _{CC} if it is not used.

a. All dedicated inputs including the CLK, DEDCLK, PLLIN, PLL_{RST}, and IOCTRL pins, are clamped to the V_{CC} rail, not the V_{CCIO}. Therefore, these pins can only be driven up to V_{CC} + 0.3 V. These input pins are LVCMOS2 compliant only (2.5 V).

b. All PLLOUT output pins are driven by the V_{CC} rail, not the V_{CCIO} rail. These output pins are LVCMOS2 compliant only (2.5 V).

Recommended Unused Pin Terminations for the EclipsePlus Devices

All unused, general purpose I/O pins can be tied to V_{CC} , GND, or HIZ (high impedance) internally using the Configuration Editor. This option is given in the bottom-right corner of the placement window. To use the Placement Editor, choose **Constraint** → **Fix Placement** in the Option pull-down menu of SpDE.

The rest of the pins should be terminated at the board level in the manner presented in **Table 24**.

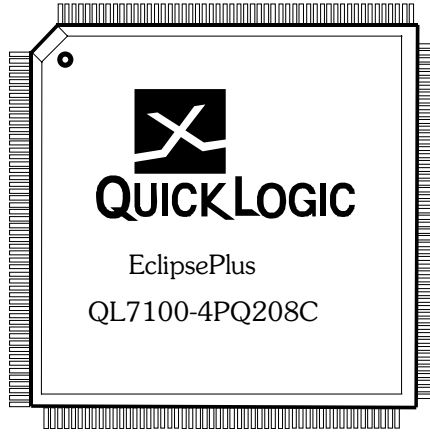
Table 24: Recommended Unused Pin Terminations

Signal Name	Recommended Termination
PLLOUT<x> ^a	Unused PLL output pins must be connected to either V_{CC} or GND so that their associated input buffer never floats. Utilized PLL output pins that route the PLL clock outside of the chip should not be tied to either V_{CC} or GND.
IOCTRL<y> ^b	Any unused pins of this type must be connected to either V_{CC} or GND.
CLK/PLLIN<x>	Any unused clock pins should be connected to V_{CC} or GND.
PLL_RST<x>	If a PLL module is not used, then the associated PLL_RST<x> must be connected to V_{CC} ; under normal operation, use it as needed. If PLLs are not used, the associated PLL_RST pin must be connected to the same voltage as V_{CCPLL} (2.5 V or GND).
INREF<y>	If an I/O bank does not require the use of INREF signal the pin should be connected to GND.

a. x represents a number.

b. y represents an alphabetical character.

QL7100 – 208 PQFP Pinout Diagram



QL7100 – 208 PQFP Pinout Table

Table 25: 208 PQFP Pinout Table

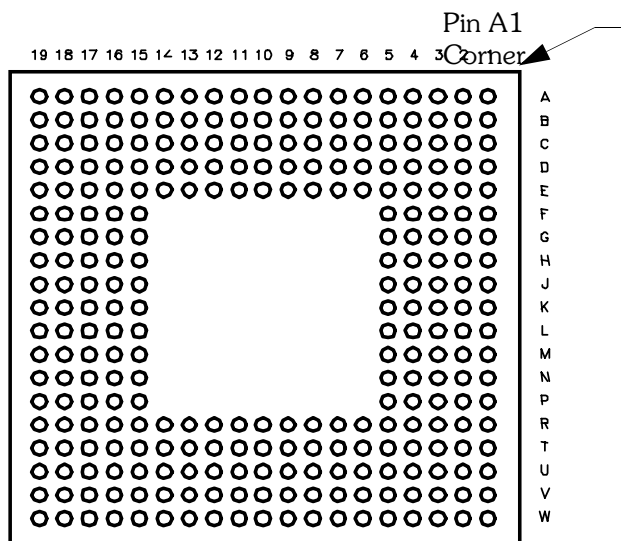
PQFP	Function	PQFP	Function	PQFP	Function	PQFP	Function	PQFP	Function
1	PLLST(3)	43	IO(B)	85	IO(D)	127	CLK(5), PLLIN(3)	169	IOCTRL(G)
2	V _{CCPLL} (3)	44	V _{CCIO} (B)	86	V _{CC}	128	CLK(6)	170	INREF(G)
3	GND	45	IO(B)	87	IO(D)	129	V _{CC}	171	IOCTRL(G)
4	GND	46	V _{CC}	88	IO(D)	130	CLK(7)	172	IO(G)
5	IO(A)	47	IO(B)	89	V _{CC}	131	V _{CC}	173	IO(G)
6	IO(A)	48	IO(B)	90	IO(D)	132	CLK(8)	174	IO(G)
7	IO(A)	49	GND	91	IO(D)	133	TMS	175	V _{CC}
8	V _{CCIO} (A)	50	TDO	92	IOCTRL(D)	134	IO(F)	176	IO(G)
9	IO(A)	51	PLLOUT(1)	93	INREF(D)	135	IO(F)	177	V _{CCIO} (G)
10	IO(A)	52	GNDPLL(2)	94	IOCTRL(D)	136	IO(F)	178	GND
11	IOCTRL(A)	53	GND	95	IO(D)	137	GND	179	IO(G)
12	V _{CC}	54	V _{CCPLL} (2)	96	IO(D)	138	V _{CCIO} (F)	180	IO(G)
13	INREF(A)	55	PLLST(2)	97	IO(D)	139	IO(F)	181	IO(G)
14	IOCTRL(A)	56	V _{CC}	98	V _{CCIO} (D)	140	IO(F)	182	V _{CC}
15	IO(A)	57	IO(C)	99	IO(D)	141	IO(F)	183	TCK
16	IO(A)	58	GND	100	IO(D)	142	IO(F)	184	V _{CC}
17	IO(A)	59	IO(C)	101	GND	143	IO(F)	185	IO(H)
18	IO(A)	60	V _{CCIO} (C)	102	PLLOUT(0)	144	IOCTRL(F)	186	IO(H)
19	V _{CCIO} (A)	61	IO(C)	103	GND	145	INREF(F)	187	IO(H)
20	IO(A)	62	IO(C)	104	GNDPLL(1)	146	V _{CC}	188	GND
21	GND	63	IO(C)	105	PLLST(1)	147	IOCTRL(F)	189	V _{CCIO} (H)
22	IO(A)	64	IO(C)	106	V _{CCPLL} (1)	148	IO(F)	190	IO(H)
23	TDI	65	IO(C)	107	IO(E)	149	IO(F)	191	IO(H)
24	CLK(0)	66	IO(C)	108	GND	150	V _{CCIO} (F)	192	IOCTRL(H)
25	CLK(1)	67	IOCTRL(C)	109	IO(E)	151	IO(F)	193	IO(H)
26	V _{CC}	68	INREF(C)	110	IO(E)	152	IO(F)	194	INREF(H)
27	CLK(2), PLLIN(2)	69	IOCTRL(C)	111	V _{CCIO} (E)	153	GND	195	V _{CC}
28	CLK(3), PLLIN(1)	70	IO(C)	112	IO(E)	154	IO(F)	196	IOCTRL(H)
29	V _{CC}	71	IO(C)	113	V _{CC}	155	PLLOUT(3)	197	IO(H)
30	CLK(4), DEDCLK, PLLIN(0)	72	V _{CCIO} (C)	114	IO(E)	156	GNDPLL(0)	198	IO(H)
31	IO(B)	73	IO(C)	115	IO(E)	157	GND	199	IO(H)
32	IO(B)	74	IO(C)	116	IO(E)	158	V _{CCPLL} (0)	200	IO(H)
33	GND	75	GND	117	IOCTRL(E)	159	PLLST(0)	201	IO(H)
34	V _{CCIO} (B)	76	V _{CC}	118	INREF(E)	160	GND	202	IO(H)
35	IO(B)	77	IO(C)	119	IOCTRL(E)	161	IO(G)	203	V _{CCIO} (H)
36	IO(B)	78	TRSTB	120	IO(E)	162	V _{CCIO} (G)	204	GND
37	IO(B)	79	V _{CC}	121	IO(E)	163	IO(G)	205	IO(H)
38	IO(B)	80	IO(D)	122	V _{CCIO} (E)	164	IO(G)	206	PLLOUT(2)
39	IOCTRL(B)	81	IO(D)	123	GND	165	V _{CC}	207	GND
40	INREF(B)	82	IO(D)	124	IO(E)	166	IO(G)	208	GNDPLL(3)
41	IOCTRL(B)	83	GND	125	IO(E)	167	IO(G)		
42	IO(B)	84	V _{CCIO} (D)	126	IO(E)	168	IO(G)		

QL7100 – 280 LFBGA Pinout Diagram

Top



Bottom



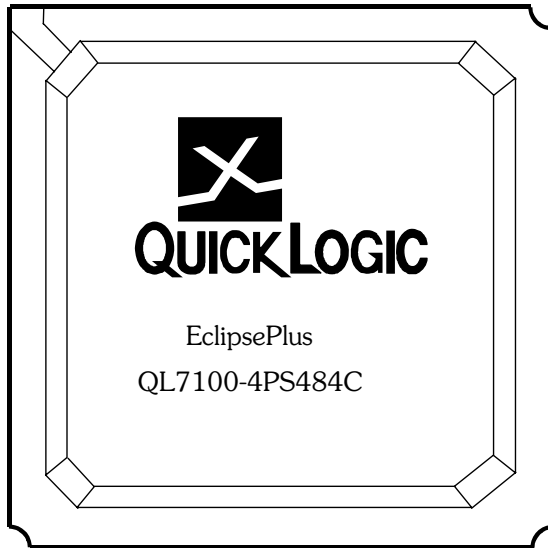
QL7100 – 280 LFBGA Pinout Table

Table 26: 280 LFBGA Pinout Table

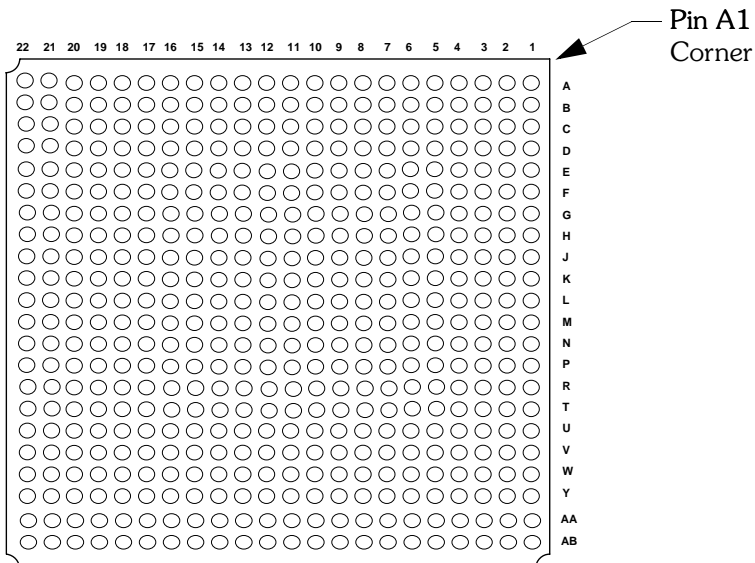
LFBGA	Function	LFBGA	Function	LFBGA	Function	LFBGA	Function	LFBGA	Function	LFBGA	Function
A1	PLLOUT(3)	C10	CLK(5)/ PLLIN(3)	E19	IOCTRL(D)	K16	I/O(C)	R4	I/O(H)	U13	I/O(B)
A2	GNDPLL(0)	C11	V _{CCIO} (E)	F1	INREF(G)	K17	I/O(D)	R5	GND	U14	IOCTRL(B)
A3	I/O(F)	C12	I/O(E)	F2	IOCTRL(G)	K18	I/O(C)	R6	GND	U15	V _{CCIO} (B)
A4	I/O(F)	C13	I/O(E)	F3	I/O(G)	K19	TRSTB	R7	V _{CC}	U16	I/O(B)
A5	I/O(F)	C14	I/O(E)	F4	I/O(G)	L1	I/O(H)	R8	V _{CC}	U17	TDO
A6	IOCTRL(F)	C15	V _{CCIO} (E)	F5	GND	L2	I/O(H)	R9	GND	U18	PLLST(2)
A7	I/O(F)	C16	I/O(E)	F15	V _{CC}	L3	V _{CCIO} (H)	R10	GND	U19	I/O(B)
A8	I/O(F)	C17	I/O(E)	F16	IOCTRL(D)	L4	I/O(H)	R11	V _{CC}	V1	PLLOUT(2)
A9	I/O(F)	C18	I/O(E)	F17	I/O(D)	L5	V _{CC}	R12	V _{CC}	V2	GNDPLL(3)
A10	CLK(7)	C19	I/O(E)	F18	I/O(D)	L15	GND	R13	V _{CC}	V3	GND
A11	I/O(E)	D1	I/O(G)	F19	I/O(D)	L16	I/O(C)	R14	V _{CC}	V4	I/O(A)
A12	I/O(E)	D2	I/O(G)	G1	I/O(G)	L17	V _{CCIO} (C)	R15	GND	V5	I/O(A)
A13	I/O(E)	D3	I/O(F)	G2	I/O(G)	L18	I/O(C)	R16	I/O(C)	V6	IOCTRL(A)
A14	IOCTRL(E)	D4	I/O(F)	G3	IOCTRL(G)	L19	I/O(C)	R17	V _{CCIO} (C)	V7	I/O(A)
A15	I/O(E)	D5	I/O(F)	G4	I/O(G)	M1	I/O(H)	R18	I/O(C)	V8	I/O(A)
A16	I/O(E)	D6	I/O(F)	G5	V _{CC}	M2	I/O(H)	R19	I/O(C)	V9	I/O(A)
A17	I/O(E)	D7	I/O(F)	G15	V _{CC}	M3	I/O(H)	T1	I/O(H)	V10	CLK(1)
A18	PLLST(1)	D8	I/O(F)	G16	I/O(D)	M4	I/O(H)	T2	I/O(H)	V11	CLK(4) DEDCLK/ PLLIN(0)
A19	GND	D9	CLK(8)	G17	I/O(D)	M5	V _{CC}	T3	I/O(A)	V12	I/O(B)
B1	PLLST(0)	D10	I/O(E)	G18	I/O(D)	M15	V _{CC}	T4	I/O(A)	V13	I/O(B)
B2	GND	D11	I/O(E)	G19	I/O(D)	M16	INREF(C)	T5	I/O(A)	V14	INREF(B)
B3	I/O(F)	D12	I/O(E)	H1	I/O(G)	M17	I/O(C)	T6	IOCTRL(A)	V15	I/O(B)
B4	I/O(F)	D13	INREF(E)	H2	I/O(G)	M18	I/O(C)	T7	I/O(A)	V16	I/O(B)
B5	I/O(F)	D14	I/O(E)	H3	I/O(G)	M19	I/O(C)	T8	I/O(A)	V17	I/O(B)
B6	INREF(F)	D15	I/O(E)	H4	I/O(G)	N1	IOCTRL(H)	T9	I/O(A)	V18	GNDPLL(2)
B7	I/O(F)	D16	I/O(D)	H5	V _{CC}	N2	I/O(H)	T10	I/O(A)	V19	GND
B8	I/O(F)	D17	I/O(D)	H15	V _{CC}	N3	I/O(H)	T11	CLK(3)/ PLLIN(1)	W1	GND
B9	TMS	D18	I/O(D)	H16	V _{CC}	N4	I/O(H)	T12	I/O(B)	W2	PLLST(3)
B10	CLK(6)	D19	I/O(D)	H17	I/O(D)	N5	V _{CC}	T13	I/O(B)	W3	I/O(A)
B11	I/O(E)	E1	I/O(G)	H18	I/O(D)	N15	V _{CC}	T14	I/O(B)	W4	I/O(A)
B12	I/O(E)	E2	I/O(G)	H19	I/O(D)	N16	I/O(C)	T15	I/O(B)	W5	I/O(A)
B13	IOCTRL(E)	E3	V _{CCIO} (G)	J1	I/O(G)	N17	I/O(C)	T16	I/O(B)	W6	I/O(A)
B14	I/O(E)	E4	I/O(F)	J2	I/O(G)	N18	IOCTRL(C)	T17	V _{CCPLL} (2)	W7	I/O(A)
B15	I/O(E)	E5	GND	J3	V _{CCIO} (G)	N19	IOCTRL(C)	T18	I/O(B)	W8	I/O(A)
B16	I/O(E)	E6	V _{CC}	J4	I/O(G)	P1	I/O(H)	T19	I/O(B)	W9	TDI
B17	V _{CCPLL} (1)	E7	V _{CC}	J5	GND	P2	I/O(H)	U1	I/O(A)	W10	CLK(2)/ PLLIN(2)
B18	GNDPLL(1)	E8	V _{CC}	J15	V _{CC}	P3	IOCTRL(H)	U2	I/O(A)	W11	I/O(B)
B19	PLLOUT(0)	E9	V _{CC}	J16	I/O(C)	P4	INREF(H)	U3	V _{CCPLL} (3)	W12	I/O(B)
C1	I/O(F)	E10	GND	J17	V _{CCIO} (D)	P5	V _{CC}	U4	I/O(A)	W13	I/O(B)
C2	V _{CCPLL} (0)	E11	GND	J18	I/O(D)	P15	GND	U5	V _{CCIO} (A)	W14	IOCTRL(B)
C3	I/O(F)	E12	V _{CC}	J19	I/O(D)	P16	I/O(C)	U6	INREF(A)	W15	I/O(B)
C4	I/O(F)	E13	V _{CC}	K1	V _{CC}	P17	I/O(C)	U7	I/O(A)	W16	I/O(B)
C5	V _{CCIO} (F)	E14	GND	K2	TCK	P18	I/O(C)	U8	I/O(A)	W17	I/O(B)
C6	IOCTRL(F)	E15	GND	K3	I/O(G)	P19	I/O(C)	U9	V _{CCIO} (A)	W18	I/O(B)
C7	I/O(F)	E16	I/O(D)	K4	I/O(G)	R1	I/O(H)	U10	CLK(0)	W19	PLLOUT(1)
C8	I/O(F)	E17	V _{CCIO} (D)	K5	GND	R2	I/O(H)	U11	V _{CCIO} (B)		
C9	V _{CCIO} (F)	E18	INREF(D)	K15	GND	R3	V _{CCIO} (H)	U12	I/O(B)		

QL7100 – 484 PBGA Pinout Diagram

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QL7100 – 484 PBGA Pinout Table

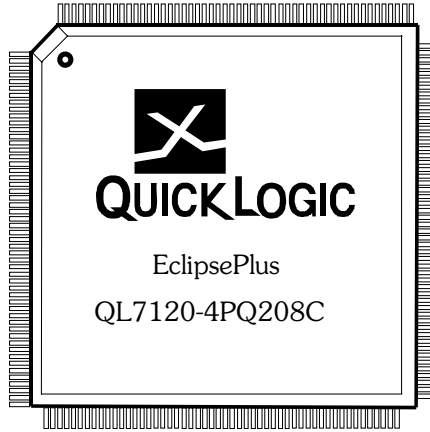
Table 27: 484 PBGA Pinout Table

PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function
A1	NC	C1	NC	E1	IOCTRL(A)	G1	NC	J1	I/O(A)	L1	CLK(4) DEDCLK/ PLLIN(0)
A2	PLLRST(3)	C2	I/O(A)	E2	I/O(A)	G2	NC	J2	I/O(A)	L2	CLK(0)
A3	I/O(A)	C3	V _{CCPLL} (3)	E3	I/O(A)	G3	I/O(A)	J3	I/O(A)	L3	CLK(2)/ PLLIN(2)
A4	I/O(A)	C4	PLLOUT(2)	E4	I/O(A)	G4	I/O(A)	J4	I/O(A)	L4	I/O(A)
A5	I/O(A)	C5	I/O(A)	E5	NC	G5	I/O(A)	J5	I/O(A)	L5	I/O(A)
A6	NC	C6	NC	E6	I/O(H)	G6	I/O(A)	J6	I/O(A)	L6	I/O(A)
A7	I/O(H)	C7	I/O(H)	E7	NC	G7	GND	J7	I/O(A)	L7	GND
A8	IOCTRL(H)	C8	NC	E8	I/O(H)	G8	I/O(H)	J8	V _{CC}	L8	GND
A9	I/O(H)	C9	IOCTRL(H)	E9	I/O(H)	G9	I/O(H)	J9	GND	L9	GND
A10	NC	C10	NC	E10	I/O(H)	G10	NC	J10	V _{CC}	L10	GND
A11	NC	C11	I/O(H)	E11	V _{CC}	G11	I/O(G)	J11	V _{CC}	L11	GND
A12	TCK	C12	NC	E12	I/O(G)	G12	GND	J12	GND	L12	GND
A13	I/O(G)	C13	I/O(G)	E13	I/O(G)	G13	NC	J13	V _{CC}	L13	GND
A14	I/O(G)	C14	NC	E14	NC	G14	NC	J14	GND	L14	V _{CC}
A15	I/O(G)	C15	I/O(G)	E15	IOCTRL(G)	G15	I/O(G)	J15	V _{CC}	L15	V _{CC}
A16	NC	C16	I/O(G)	E16	I/O(G)	G16	GND	J16	I/O(F)	L16	CLK(6)
A17	I/O(G)	C17	NC	E17	INREF(G)	G17	V _{CCIO} (F)	J17	V _{CCIO} (F)	L17	V _{CCIO} (F)
A18	I/O(G)	C18	I/O(G)	E18	NC	G18	I/O(F)	J18	I/O(F)	L18	I/O(F)
A19	I/O(F)	C19	I/O(F)	E19	I/O(F)	G19	I/O(F)	J19	I/O(F)	L19	CLK(8)
A20	GND	C20	GNDPLL(0)	E20	I/O(F)	G20	I/O(F)	J20	I/O(F)	L20	I/O(F)
A21	PLLOUT(3)	C21	I/O(F)	E21	NC	G21	INREF(F)	J21	I/O(F)	L21	NC
A22	I/O(F)	C22	I/O(F)	E22	I/O(F)	G22	I/O(F)	J22	I/O(F)	L22	I/O(F)
B1	I/O(A)	D1	I/O(A)	F1	I/O(A)	H1	I/O(A)	K1	TDI	M1	I/O(B)
B2	GND	D2	I/O(A)	F2	INREF(A)	H2	I/O(A)	K2	I/O(A)	M2	I/O(B)
B3	GNDPLL(3)	D3	I/O(A)	F3	NC	H3	I/O(A)	K3	I/O(A)	M3	I/O(B)
B4	GND	D4	I/O(A)	F4	I/O(A)	H4	I/O(A)	K4	I/O(A)	M4	CLK(3)/ PLLIN(1)
B5	I/O(A)	D5	I/O(A)	F5	I/O(A)	H5	IOCTRL(A)	K5	I/O(A)	M5	NC
B6	I/O(H)	D6	I/O(H)	F6	V _{CCIO} (A)	H6	V _{CCIO} (A)	K6	V _{CCIO} (A)	M6	V _{CCIO} (B)
B7	I/O(H)	D7	NC	F7	V _{CCIO} (H)	H7	I/O(H)	K7	NC	M7	CLK(1)
B8	INREF(H)	D8	I/O(H)	F8	I/O(H)	H8	GND	K8	V _{CC}	M8	V _{CC}
B9	I/O(H)	D9	NC	F9	V _{CCIO} (H)	H9	V _{CC}	K9	V _{CC}	M9	V _{CC}
B10	I/O(H)	D10	I/O(H)	F10	I/O(H)	H10	V _{CC}	K10	GND	M10	GND
B11	I/O(H)	D11	I/O(H)	F11	V _{CCIO} (H)	H11	V _{CC}	K11	GND	M11	GND
B12	NC	D12	I/O(G)	F12	V _{CCIO} (G)	H12	GND	K12	GND	M12	GND
B13	NC	D13	I/O(G)	F13	I/O(G)	H13	V _{CC}	K13	GND	M13	GND
B14	NC	D14	I/O(G)	F14	V _{CCIO} (G)	H14	V _{CC}	K14	V _{CC}	M14	GND
B15	NC	D15	IOCTRL(G)	F15	NC	H15	GND	K15	V _{CC}	M15	GND
B16	I/O(G)	D16	I/O(G)	F16	V _{CCIO} (G)	H16	I/O(F)	K16	NC	M16	GND
B17	I/O(G)	D17	I/O(G)	F17	NC	H17	I/O(F)	K17	I/O(F)	M17	I/O(E)
B18	I/O(G)	D18	I/O(F)	F18	I/O(F)	H18	NC	K18	I/O(F)	M18	I/O(E)
B19	PLLRST(0)	D19	V _{CCPLL} (0)	F19	I/O(F)	H19	I/O(F)	K19	NC	M19	I/O(E)
B20	I/O(F)	D20	I/O(F)	F20	IOCTRL(F)	H20	I/O(F)	K20	I/O(F)	M20	CLK(7)
B21	I/O(F)	D21	I/O(F)	F21	I/O(F)	H21	I/O(F)	K21	I/O(F)	M21	CLK(5)/ PLLIN(3)
B22	I/O(F)	D22	I/O(F)	F22	IOCTRL(F)	H22	NC	K22	NC	M22	TMS

Table 27: 484 PBGA Pinout Table (Continued)

PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function
N1	NC	P16	I/O(E)	T9	NC	V2	I/O(B)	W17	NC	AA10	I/O(C)
N2	I/O(B)	P17	NC	T10	TRSTB	V3	I/O(B)	W18	I/O(E)	AA11	I/O(C)
N3	I/O(B)	P18	I/O(E)	T11	GND	V4	I/O(B)	W19	NC	AA12	I/O(D)
N4	NC	P19	NC	T12	NC	V5	I/O(B)	W20	I/O(E)	AA13	I/O(D)
N5	I/O(B)	P20	I/O(E)	T13	I/O(D)	V6	NC	W21	NC	AA14	I/O(D)
N6	NC	P21	I/O(E)	T14	NC	V7	I/O(C)	W22	I/O(E)	AA15	I/O(D)
N7	NC	P22	I/O(E)	T15	I/O(D)	V8	I/O(C)	Y1	I/O(B)	AA16	NC
N8	V _{CC}	R1	I/O(B)	T16	GND	V9	NC	Y2	I/O(B)	AA17	NC
N9	V _{CC}	R2	INREF(B)	T17	I/O(E)	V10	I/O(C)	Y3	V _{CCPLL(2)}	AA18	I/O(D)
N10	GND	R3	I/O(B)	T18	I/O(E)	V11	NC	Y4	I/O(C)	AA19	I/O(E)
N11	GND	R4	I/O(B)	T19	NC	V12	V _{CC}	Y5	I/O(C)	AA20	GNDPLL(1)
N12	GND	R5	I/O(B)	T20	NC	V13	NC	Y6	I/O(C)	AA21	I/O(E)
N13	GND	R6	NC	T21	IOCTRL(E)	V14	I/O(D)	Y7	I/O(C)	AA22	I/O(E)
N14	V _{CC}	R7	I/O(B)	T22	I/O(E)	V15	I/O(D)	Y8	IOCTRL(C)	AB1	I/O(B)
N15	V _{CC}	R8	GND	U1	IOCTRL(B)	V16	INREF(D)	Y9	I/O(C)	AB2	GNDPLL(2)
N16	I/O(E)	R9	V _{CC}	U2	I/O(B)	V17	I/O(D)	Y10	I/O(C)	AB3	PLLRSST(2)
N17	V _{CCIO(E)}	R10	V _{CC}	U3	IOCTRL(B)	V18	I/O(E)	Y11	I/O(D)	AB4	I/O(B)
N18	I/O(E)	R11	GND	U4	I/O(B)	V19	I/O(E)	Y12	NC	AB5	I/O(B)
N19	I/O(E)	R12	V _{CC}	U5	I/O(B)	V20	I/O(E)	Y13	NC	AB6	I/O(C)
N20	I/O(E)	R13	V _{CC}	U6	I/O(C)	V21	I/O(E)	Y14	I/O(D)	AB7	I/O(C)
N21	I/O(E)	R14	V _{CC}	U7	V _{CCIO(C)}	V22	I/O(E)	Y15	IOCTRL(D)	AB8	IOCTRL(C)
N22	I/O(E)	R15	GND	U8	NC	W1	I/O(B)	Y16	I/O(D)	AB9	I/O(C)
P1	NC	R16	I/O(D)	U9	V _{CCIO(C)}	W2	I/O(B)	Y17	I/O(D)	AB10	I/O(C)
P2	I/O(B)	R17	V _{CCIO(E)}	U10	I/O(C)	W3	I/O(B)	Y18	I/O(E)	AB11	NC
P3	I/O(B)	R18	I/O(E)	U11	V _{CCIO(C)}	W4	I/O(B)	Y19	PLLOUT(0)	AB12	I/O(D)
P4	I/O(B)	R19	I/O(E)	U12	V _{CCIO(D)}	W5	I/O(B)	Y20	PLLRSST(1)	AB13	I/O(D)
P5	I/O(B)	R20	I/O(E)	U13	I/O(D)	W6	I/O(C)	Y21	I/O(E)	AB14	NC
P6	V _{CCIO(B)}	R21	I/O(E)	U14	V _{CCIO(D)}	W7	NC	Y22	I/O(E)	AB15	I/O(D)
P7	I/O(B)	R22	I/O(E)	U15	NC	W8	NC	AA1	TDO	AB16	IOCTRL(D)
P8	V _{CC}	T1	I/O(B)	U16	V _{CCIO(D)}	W9	NC	AA2	PLLOUT(1)	AB17	I/O(D)
P9	GND	T2	I/O(B)	U17	V _{CCIO(E)}	W10	NC	AA3	GND	AB18	I/O(D)
P10	V _{CC}	T3	I/O(B)	U18	I/O(E)	W11	I/O(C)	AA4	I/O(B)	AB19	I/O(E)
P11	GND	T4	I/O(B)	U19	I/O(E)	W12	NC	AA5	I/O(C)	AB20	GND
P12	V _{CC}	T5	I/O(B)	U20	IOCTRL(E)	W13	I/O(D)	AA6	I/O(C)	AB21	V _{CCPLL(1)}
P13	V _{CC}	T6	V _{CCIO(B)}	U21	NC	W14	NC	AA7	NC	AB22	I/O(E)
P14	GND	T7	GND	U22	INREF(E)	W15	I/O(D)	AA8	INREF(C)		
P15	V _{CC}	T8	I/O(C)	V1	I/O(B)	W16	NC	AA9	NC		

QL7120 – 208 PQFP Pinout Diagram



QL7120 – 208 PQFP Pinout Table

Table 28: 208 PQFP Pinout Table

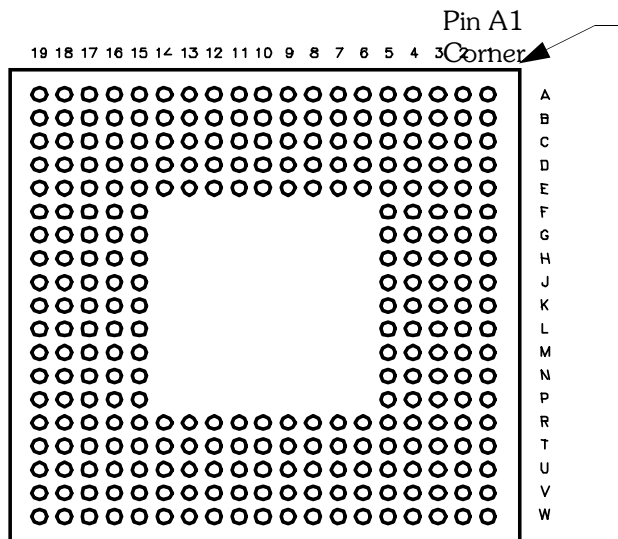
PQFP	Function	PQFP	Function	PQFP	Function	PQFP	Function	PQFP	Function
1	PLLST(3)	43	IO(B)	85	IO(D)	127	CLK(5), PLLIN(3)	169	IOCTRL(G)
2	V _{CCPLL} (3)	44	V _{CCIO} (B)	86	V _{CC}	128	CLK(6)	170	INREF(G)
3	GND	45	IO(B)	87	IO(D)	129	V _{CC}	171	IOCTRL(G)
4	GND	46	V _{CC}	88	IO(D)	130	CLK(7)	172	IO(G)
5	IO(A)	47	IO(B)	89	V _{CC}	131	V _{CC}	173	IO(G)
6	IO(A)	48	IO(B)	90	IO(D)	132	CLK(8)	174	IO(G)
7	IO(A)	49	GND	91	IO(D)	133	TMS	175	V _{CC}
8	V _{CCIO} (A)	50	TDO	92	IOCTRL(D)	134	IO(F)	176	IO(G)
9	IO(A)	51	PLLOUT(1)	93	INREF(D)	135	IO(F)	177	V _{CCIO} (G)
10	IO(A)	52	GNDPLL(2)	94	IOCTRL(D)	136	IO(F)	178	GND
11	IOCTRL(A)	53	GND	95	IO(D)	137	GND	179	IO(G)
12	V _{CC}	54	V _{CCPLL} (2)	96	IO(D)	138	V _{CCIO} (F)	180	IO(G)
13	INREF(A)	55	PLLST(2)	97	IO(D)	139	IO(F)	181	IO(G)
14	IOCTRL(A)	56	V _{CC}	98	V _{CCIO} (D)	140	IO(F)	182	V _{CC}
15	IO(A)	57	IO(C)	99	IO(D)	141	IO(F)	183	TCK
16	IO(A)	58	GND	100	IO(D)	142	IO(F)	184	V _{CC}
17	IO(A)	59	IO(C)	101	GND	143	IO(F)	185	IO(H)
18	IO(A)	60	V _{CCIO} (C)	102	PLLOUT(0)	144	IOCTRL(F)	186	IO(H)
19	V _{CCIO} (A)	61	IO(C)	103	GND	145	INREF(F)	187	IO(H)
20	IO(A)	62	IO(C)	104	GNDPLL(1)	146	V _{CC}	188	GND
21	GND	63	IO(C)	105	PLLST(1)	147	IOCTRL(F)	189	V _{CCIO} (H)
22	IO(A)	64	IO(C)	106	V _{CCPLL} (1)	148	IO(F)	190	IO(H)
23	TDI	65	IO(C)	107	IO(E)	149	IO(F)	191	IO(H)
24	CLK(0)	66	IO(C)	108	GND	150	V _{CCIO} (F)	192	IOCTRL(H)
25	CLK(1)	67	IOCTRL(C)	109	IO(E)	151	IO(F)	193	IO(H)
26	V _{CC}	68	INREF(C)	110	IO(E)	152	IO(F)	194	INREF(H)
27	CLK(2), PLLIN(2)	69	IOCTRL(C)	111	V _{CCIO} (E)	153	GND	195	V _{CC}
28	CLK(3), PLLIN(1)	70	IO(C)	112	IO(E)	154	IO(F)	196	IOCTRL(H)
29	V _{CC}	71	IO(C)	113	V _{CC}	155	PLLOUT(3)	197	IO(H)
30	CLK(4), DEDCLK, PLLIN(0)	72	V _{CCIO} (C)	114	IO(E)	156	GNDPLL(0)	198	IO(H)
31	IO(B)	73	IO(C)	115	IO(E)	157	GND	199	IO(H)
32	IO(B)	74	IO(C)	116	IO(E)	158	V _{CCPLL} (0)	200	IO(H)
33	GND	75	GND	117	IOCTRL(E)	159	PLLST(0)	201	IO(H)
34	V _{CCIO} (B)	76	V _{CC}	118	INREF(E)	160	GND	202	IO(H)
35	IO(B)	77	IO(C)	119	IOCTRL(E)	161	IO(G)	203	V _{CCIO} (H)
36	IO(B)	78	TRSTB	120	IO(E)	162	V _{CCIO} (G)	204	GND
37	IO(B)	79	V _{CC}	121	IO(E)	163	IO(G)	205	IO(H)
38	IO(B)	80	IO(D)	122	V _{CCIO} (E)	164	IO(G)	206	PLLOUT(2)
39	IOCTRL(B)	81	IO(D)	123	GND	165	V _{CC}	207	GND
40	INREF(B)	82	IO(D)	124	IO(E)	166	IO(G)	208	GNDPLL(3)
41	IOCTRL(B)	83	GND	125	IO(E)	167	IO(G)		
42	IO(B)	84	V _{CCIO} (D)	126	IO(E)	168	IO(G)		

QL7120 – 280 PBGA Pinout Diagram

Top



Bottom



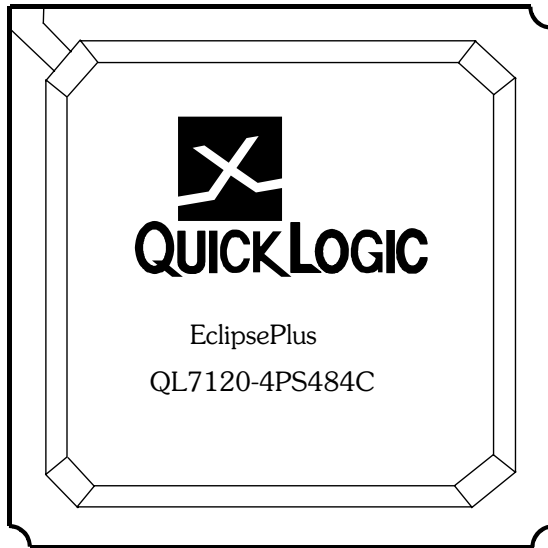
QL7120 – 280 LFBGA Pinout Table

Table 29: 280 LFBGA Pinout Table

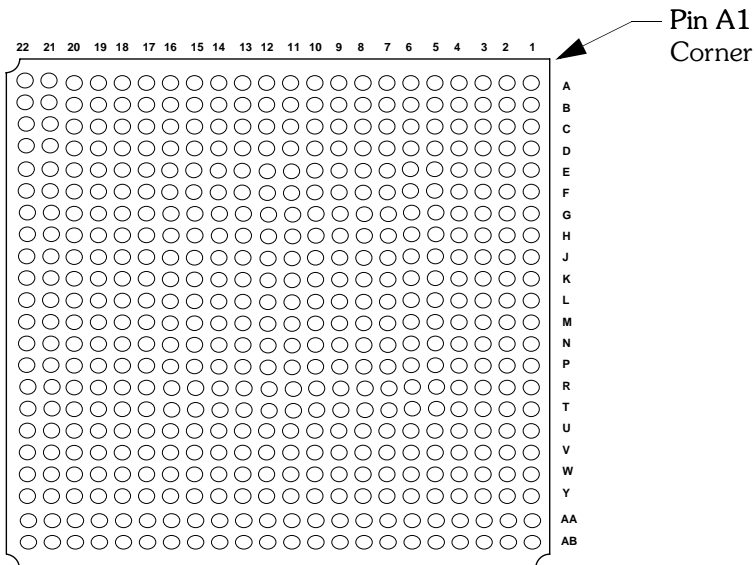
LFBGA	Function	LFBGA	Function	LFBGA	Function	LFBGA	Function	LFBGA	Function	LFBGA	Function
A1	PLLOUT(3)	C10	CLK(5) / PLLIN(3)	E19	IOCTRL(D)	K16	I/O(C)	R4	I/O(H)	U13	I/O(B)
A2	GNDPLL(0)	C11	V _{CCIO} (E)	F1	INREF(G)	K17	I/O(D)	R5	GND	U14	IOCTRL(B)
A3	I/O(F)	C12	I/O(E)	F2	IOCTRL(G)	K18	I/O(C)	R6	GND	U15	V _{CCIO} (B)
A4	I/O(F)	C13	I/O(E)	F3	I/O(G)	K19	TRSTB	R7	V _{CC}	U16	I/O(B)
A5	I/O(F)	C14	I/O(E)	F4	I/O(G)	L1	I/O(H)	R8	V _{CC}	U17	TDO
A6	IOCTRL(F)	C15	V _{CCIO} (E)	F5	GND	L2	I/O(H)	R9	GND	U18	PLLST(2)
A7	I/O(F)	C16	I/O(E)	F15	V _{CC}	L3	V _{CCIO} (H)	R10	GND	U19	I/O(B)
A8	I/O(F)	C17	I/O(E)	F16	IOCTRL(D)	L4	I/O(H)	R11	V _{CC}	V1	PLLOUT(2)
A9	I/O(F)	C18	I/O(E)	F17	I/O(D)	L5	V _{CC}	R12	V _{CC}	V2	GNDPLL(3)
A10	CLK(7)	C19	I/O(E)	F18	I/O(D)	L15	GND	R13	V _{CC}	V3	GND
A11	I/O(E)	D1	I/O(G)	F19	I/O(D)	L16	I/O(C)	R14	V _{CC}	V4	I/O(A)
A12	I/O(E)	D2	I/O(G)	G1	I/O(G)	L17	V _{CCIO} (C)	R15	GND	V5	I/O(A)
A13	I/O(E)	D3	I/O(F)	G2	I/O(G)	L18	I/O(C)	R16	I/O(C)	V6	IOCTRL(A)
A14	IOCTRL(E)	D4	I/O(F)	G3	IOCTRL(G)	L19	I/O(C)	R17	V _{CCIO} (C)	V7	I/O(A)
A15	I/O(E)	D5	I/O(F)	G4	I/O(G)	M1	I/O(H)	R18	I/O(C)	V8	I/O(A)
A16	I/O(E)	D6	I/O(F)	G5	V _{CC}	M2	I/O(H)	R19	I/O(C)	V9	I/O(A)
A17	I/O(E)	D7	I/O(F)	G15	V _{CC}	M3	I/O(H)	T1	I/O(H)	V10	CLK(1)
A18	PLLST(1)	D8	I/O(F)	G16	I/O(D)	M4	I/O(H)	T2	I/O(H)	V11	CLK(4) DEDCLK/ PLLIN(0)
A19	GND	D9	CLK(8)	G17	I/O(D)	M5	V _{CC}	T3	I/O(A)	V12	I/O(B)
B1	PLLST(0)	D10	I/O(E)	G18	I/O(D)	M15	V _{CC}	T4	I/O(A)	V13	I/O(B)
B2	GND	D11	I/O(E)	G19	I/O(D)	M16	INREF(C)	T5	I/O(A)	V14	INREF(B)
B3	I/O(F)	D12	I/O(E)	H1	I/O(G)	M17	I/O(C)	T6	IOCTRL(A)	V15	I/O(B)
B4	I/O(F)	D13	INREF(E)	H2	I/O(G)	M18	I/O(C)	T7	I/O(A)	V16	I/O(B)
B5	I/O(F)	D14	I/O(E)	H3	I/O(G)	M19	I/O(C)	T8	I/O(A)	V17	I/O(B)
B6	INREF(F)	D15	I/O(E)	H4	I/O(G)	N1	IOCTRL(H)	T9	I/O(A)	V18	GNDPLL(2)
B7	I/O(F)	D16	I/O(D)	H5	V _{CC}	N2	I/O(H)	T10	I/O(A)	V19	GND
B8	I/O(F)	D17	I/O(D)	H15	V _{CC}	N3	I/O(H)	T11	CLK(3)/ PLLIN(1)	W1	GND
B9	TMS	D18	I/O(D)	H16	V _{CC}	N4	I/O(H)	T12	I/O(B)	W2	PLLST(3)
B10	CLK(6)	D19	I/O(D)	H17	I/O(D)	N5	V _{CC}	T13	I/O(B)	W3	I/O(A)
B11	I/O(E)	E1	I/O(G)	H18	I/O(D)	N15	V _{CC}	T14	I/O(B)	W4	I/O(A)
B12	I/O(E)	E2	I/O(G)	H19	I/O(D)	N16	I/O(C)	T15	I/O(B)	W5	I/O(A)
B13	IOCTRL(E)	E3	V _{CCIO} (G)	J1	I/O(G)	N17	I/O(C)	T16	I/O(B)	W6	I/O(A)
B14	I/O(E)	E4	I/O(F)	J2	I/O(G)	N18	IOCTRL(C)	T17	V _{CCPLL} (2)	W7	I/O(A)
B15	I/O(E)	E5	GND	J3	V _{CCIO} (G)	N19	IOCTRL(C)	T18	I/O(B)	W8	I/O(A)
B16	I/O(E)	E6	V _{CC}	J4	I/O(G)	P1	I/O(H)	T19	I/O(B)	W9	TDI
B17	V _{CCPLL} (1)	E7	V _{CC}	J5	GND	P2	I/O(H)	U1	I/O(A)	W10	CLK(2)/ PLLIN(2)
B18	GNDPLL(1)	E8	V _{CC}	J15	V _{CC}	P3	IOCTRL(H)	U2	I/O(A)	W11	I/O(B)
B19	PLLOUT(0)	E9	V _{CC}	J16	I/O(C)	P4	INREF(H)	U3	V _{CCPLL} (3)	W12	I/O(B)
C1	I/O(F)	E10	GND	J17	V _{CCIO} (D)	P5	V _{CC}	U4	I/O(A)	W13	I/O(B)
C2	V _{CCPLL} (0)	E11	GND	J18	I/O(D)	P15	GND	U5	V _{CCIO} (A)	W14	IOCTRL(B)
C3	I/O(F)	E12	V _{CC}	J19	I/O(D)	P16	I/O(C)	U6	INREF(A)	W15	I/O(B)
C4	I/O(F)	E13	V _{CC}	K1	V _{CC}	P17	I/O(C)	U7	I/O(A)	W16	I/O(B)
C5	V _{CCIO} (F)	E14	GND	K2	TCK	P18	I/O(C)	U8	I/O(A)	W17	I/O(B)
C6	IOCTRL(F)	E15	GND	K3	I/O(G)	P19	I/O(C)	U9	V _{CCIO} (A)	W18	I/O(B)
C7	I/O(F)	E16	I/O(D)	K4	I/O(G)	R1	I/O(H)	U10	CLK(0)	W19	PLLOUT(1)
C8	I/O(F)	E17	V _{CCIO} (D)	K5	GND	R2	I/O(H)	U11	V _{CCIO} (B)		
C9	V _{CCIO} (F)	E18	INREF(D)	K15	GND	R3	V _{CCIO} (H)	U12	I/O(B)		

QL7120 – 484 PBGA Pinout Diagram

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Bottom



QL7120 – 484 PBGA Pinout Table

Table 30: 484 PBGA Pinout Table

PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function
A1	I/O(A)	C1	I/O(A)	E1	IOCTRL(A)	G1	I/O(A)	J1	I/O(A)	L1	CLK(4) DEDCLK/ PLLIN(0)
A2	PLLRS(3)	C2	I/O(A)	E2	I/O(A)	G2	I/O(A)	J2	I/O(A)	L2	CLK(0)
A3	I/O(A)	C3	V _{CCPLL} (3)	E3	I/O(A)	G3	I/O(A)	J3	I/O(A)	L3	CLK(2)/ PLLIN(2)
A4	I/O(A)	C4	PLLOUT(2)	E4	I/O(A)	G4	I/O(A)	J4	I/O(A)	L4	I/O(A)
A5	I/O(A)	C5	I/O(A)	E5	I/O(A)	G5	I/O(A)	J5	I/O(A)	L5	I/O(A)
A6	I/O(H)	C6	I/O(H)	E6	I/O(H)	G6	I/O(A)	J6	I/O(A)	L6	I/O(A)
A7	I/O(H)	C7	I/O(H)	E7	N/C	G7	GND	J7	I/O(A)	L7	GND
A8	IOCTRL(H)	C8	I/O(H)	E8	I/O(H)	G8	I/O(H)	J8	V _{CC}	L8	GND
A9	I/O(H)	C9	IOCTRL(H)	E9	I/O(H)	G9	I/O(H)	J9	GND	L9	GND
A10	N/C	C10	I/O(H)	E10	I/O(H)	G10	I/O(H)	J10	V _{CC}	L10	GND
A11	N/C	C11	I/O(H)	E11	V _{CC}	G11	I/O(G)	J11	V _{CC}	L11	GND
A12	TCK	C12	I/O(H)	E12	I/O(G)	G12	GND	J12	GND	L12	GND
A13	I/O(G)	C13	I/O(G)	E13	I/O(G)	G13	I/O(G)	J13	V _{CC}	L13	GND
A14	I/O(G)	C14	I/O(G)	E14	I/O(G)	G14	I/O(G)	J14	GND	L14	V _{CC}
A15	I/O(G)	C15	I/O(G)	E15	IOCTRL(G)	G15	I/O(G)	J15	V _{CC}	L15	V _{CC}
A16	I/O(G)	C16	I/O(G)	E16	I/O(G)	G16	GND	J16	I/O(F)	L16	CLK(6)
A17	I/O(G)	C17	I/O(G)	E17	INREF(G)	G17	V _{CCIO} (F)	J17	V _{CCIO} (F)	L17	V _{CCIO} (F)
A18	I/O(G)	C18	I/O(G)	E18	I/O(G)	G18	I/O(F)	J18	I/O(F)	L18	I/O(F)
A19	I/O(F)	C19	I/O(F)	E19	I/O(F)	G19	I/O(F)	J19	I/O(F)	L19	CLK(8)
A20	GND	C20	GNDPLL(0)	E20	I/O(F)	G20	I/O(F)	J20	I/O(F)	L20	I/O(F)
A21	PLLOUT(3)	C21	I/O(F)	E21	I/O(F)	G21	INREF(F)	J21	I/O(F)	L21	I/O(F)
A22	I/O(F)	C22	I/O(F)	E22	I/O(F)	G22	I/O(F)	J22	I/O(F)	L22	I/O(F)
B1	I/O(A)	D1	I/O(A)	F1	I/O(A)	H1	I/O(A)	K1	TDI	M1	I/O(B)
B2	GND	D2	I/O(A)	F2	INREF(A)	H2	I/O(A)	K2	I/O(A)	M2	I/O(B)
B3	GNDPLL(3)	D3	I/O(A)	F3	I/O(A)	H3	I/O(A)	K3	I/O(A)	M3	I/O(B)
B4	GND	D4	I/O(A)	F4	I/O(A)	H4	I/O(A)	K4	I/O(A)	M4	CLK(3)/ PLLIN(1)
B5	I/O(A)	D5	I/O(A)	F5	I/O(A)	H5	IOCTRL(A)	K5	I/O(A)	M5	I/O(B)
B6	I/O(H)	D6	I/O(H)	F6	V _{CCIO} (A)	H6	V _{CCIO} (A)	K6	V _{CCIO} (A)	M6	V _{CCIO} (B)
B7	I/O(H)	D7	I/O(H)	F7	V _{CCIO} (H)	H7	I/O(H)	K7	I/O(A)	M7	CLK(1)
B8	INREF(H)	D8	I/O(H)	F8	I/O(H)	H8	GND	K8	V _{CC}	M8	V _{CC}
B9	I/O(H)	D9	I/O(H)	F9	V _{CCIO} (H)	H9	V _{CC}	K9	V _{CC}	M9	V _{CC}
B10	I/O(H)	D10	I/O(H)	F10	I/O(H)	H10	V _{CC}	K10	GND	M10	GND
B11	I/O(H)	D11	I/O(H)	F11	V _{CCIO} (H)	H11	V _{CC}	K11	GND	M11	GND
B12	N/C	D12	I/O(G)	F12	V _{CCIO} (G)	H12	GND	K12	GND	M12	GND
B13	N/C	D13	I/O(G)	F13	I/O(G)	H13	V _{CC}	K13	GND	M13	GND
B14	N/C	D14	I/O(G)	F14	V _{CCIO} (G)	H14	V _{CC}	K14	V _{CC}	M14	GND
B15	I/O(G)	D15	IOCTRL(G)	F15	N/C	H15	GND	K15	V _{CC}	M15	GND
B16	I/O(G)	D16	I/O(G)	F16	V _{CCIO} (G)	H16	I/O(F)	K16	I/O(F)	M16	GND
B17	I/O(G)	D17	I/O(G)	F17	N/C	H17	I/O(F)	K17	I/O(F)	M17	I/O(E)
B18	I/O(G)	D18	I/O(F)	F18	I/O(F)	H18	I/O(F)	K18	I/O(F)	M18	I/O(E)
B19	PLLRS(0)	D19	V _{CCPLL} (0)	F19	I/O(F)	H19	I/O(F)	K19	I/O(F)	M19	I/O(E)
B20	I/O(F)	D20	I/O(F)	F20	IOCTRL(F)	H20	I/O(F)	K20	I/O(F)	M20	CLK(7)
B21	I/O(F)	D21	I/O(F)	F21	I/O(F)	H21	I/O(F)	K21	I/O(F)	M21	CLK(5)/PLLIN (3)
B22	I/O(F)	D22	I/O(F)	F22	IOCTRL(F)	H22	I/O(F)	K22	I/O(F)	M22	TMS

Table 30: 484 PBGA Pinout Table (Continued)

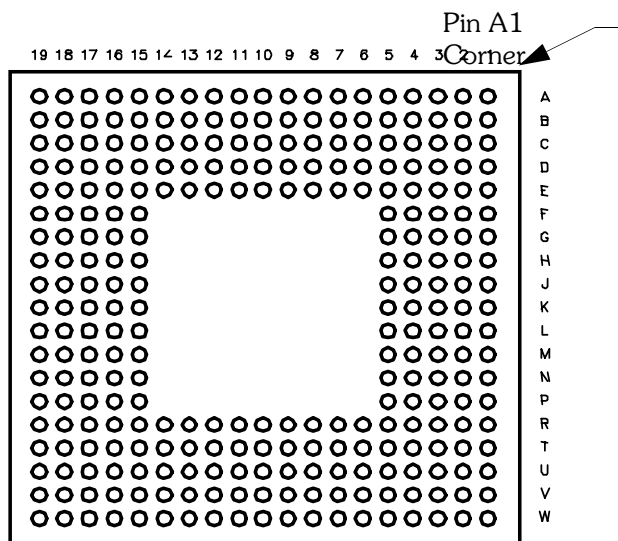
PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function
N1	I/O(B)	P16	I/O(E)	T9	N/C	V2	I/O(B)	W17	I/O(D)	AA10	I/O(C)
N2	I/O(B)	P17	I/O(E)	T10	TRSTB	V3	I/O(B)	W18	I/O(E)	AA11	I/O(C)
N3	I/O(B)	P18	I/O(E)	T11	GND	V4	I/O(B)	W19	I/O(E)	AA12	I/O(D)
N4	I/O(B)	P19	I/O(E)	T12	N/C	V5	I/O(B)	W20	I/O(E)	AA13	I/O(D)
N5	I/O(B)	P20	I/O(E)	T13	I/O(D)	V6	I/O(C)	W21	I/O(E)	AA14	I/O(D)
N6	I/O(B)	P21	I/O(E)	T14	N/C	V7	I/O(C)	W22	I/O(E)	AA15	I/O(D)
N7	I/O(B)	P22	I/O(E)	T15	I/O(D)	V8	I/O(C)	Y1	I/O(B)	AA16	I/O(D)
N8	V _{CC}	R1	I/O(B)	T16	GND	V9	N/C	Y2	I/O(B)	AA17	I/O(D)
N9	V _{CC}	R2	INREF(B)	T17	I/O(E)	V10	I/O(C)	Y3	V _{CCPLL(2)}	AA18	I/O(D)
N10	GND	R3	I/O(B)	T18	I/O(E)	V11	I/O(C)	Y4	I/O(C)	AA19	I/O(E)
N11	GND	R4	I/O(B)	T19	I/O(E)	V12	V _{CC}	Y5	I/O(C)	AA20	GNDPLL(1)
N12	GND	R5	I/O(B)	T20	I/O(E)	V13	N/C	Y6	I/O(C)	AA21	I/O(E)
N13	GND	R6	I/O(B)	T21	IOCTRL(E)	V14	I/O(D)	Y7	I/O(C)	AA22	I/O(E)
N14	V _{CC}	R7	I/O(B)	T22	I/O(E)	V15	I/O(D)	Y8	IOCTRL(C)	AB1	I/O(B)
N15	V _{CC}	R8	GND	U1	IOCTRL(B)	V16	INREF(D)	Y9	I/O(C)	AB2	GNDPLL(2)
N16	I/O(E)	R9	V _{CC}	U2	I/O(B)	V17	I/O(D)	Y10	I/O(C)	AB3	PLL RST(2)
N17	V _{CCIO(E)}	R10	V _{CC}	U3	IOCTRL(B)	V18	I/O(E)	Y11	I/O(D)	AB4	I/O(B)
N18	I/O(E)	R11	GND	U4	I/O(B)	V19	I/O(E)	Y12	I/O(D)	AB5	I/O(B)
N19	I/O(E)	R12	V _{CC}	U5	I/O(B)	V20	I/O(E)	Y13	I/O(D)	AB6	I/O(C)
N20	I/O(E)	R13	V _{CC}	U6	I/O(C)	V21	I/O(E)	Y14	I/O(D)	AB7	I/O(C)
N21	I/O(E)	R14	V _{CC}	U7	V _{CCIO(C)}	V22	I/O(E)	Y15	IOCTRL(D)	AB8	IOCTRL(C)
N22	I/O(E)	R15	GND	U8	N/C	W1	I/O(B)	Y16	I/O(D)	AB9	I/O(C)
P1	I/O(B)	R16	I/O(D)	U9	V _{CCIO(C)}	W2	I/O(B)	Y17	I/O(D)	AB10	I/O(C)
P2	I/O(B)	R17	V _{CCIO(E)}	U10	I/O(C)	W3	I/O(B)	Y18	I/O(E)	AB11	I/O(C)
P3	I/O(B)	R18	I/O(E)	U11	V _{CCIO(C)}	W4	I/O(B)	Y19	PLLOUT(0)	AB12	I/O(D)
P4	I/O(B)	R19	I/O(E)	U12	V _{CCIO(D)}	W5	I/O(B)	Y20	PLL RST(1)	AB13	I/O(D)
P5	I/O(B)	R20	I/O(E)	U13	I/O(D)	W6	I/O(C)	Y21	I/O(E)	AB14	I/O(D)
P6	V _{CCIO(B)}	R21	I/O(E)	U14	V _{CCIO(D)}	W7	N/C	Y22	I/O(E)	AB15	I/O(D)
P7	I/O(B)	R22	I/O(E)	U15	N/C	W8	I/O(C)	AA1	TDO	AB16	IOCTRL(D)
P8	V _{CC}	T1	I/O(B)	U16	V _{CCIO(D)}	W9	I/O(C)	AA2	PLLOUT(1)	AB17	I/O(D)
P9	GND	T2	I/O(B)	U17	V _{CCIO(E)}	W10	I/O(C)	AA3	GND	AB18	I/O(D)
P10	V _{CC}	T3	I/O(B)	U18	I/O(E)	W11	I/O(C)	AA4	I/O(B)	AB19	I/O(E)
P11	GND	T4	I/O(B)	U19	I/O(E)	W12	I/O(D)	AA5	I/O(C)	AB20	GND
P12	V _{CC}	T5	I/O(B)	U20	IOCTRL(E)	W13	I/O(D)	AA6	I/O(C)	AB21	V _{CCPLL(1)}
P13	V _{CC}	T6	V _{CCIO(B)}	U21	I/O(E)	W14	I/O(D)	AA7	I/O(C)	AB22	I/O(E)
P14	GND	T7	GND	U22	INREF(E)	W15	I/O(D)	AA8	INREF(C)		
P15	V _{CC}	T8	I/O(C)	V1	I/O(B)	W16	N/C	AA9	I/O(C)		

QL7160 – 280 LFBGA Pinout Diagram

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Bottom



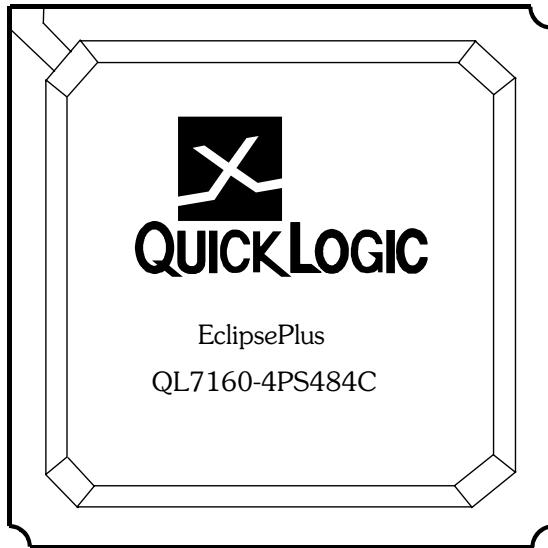
QL7160 – 280 LFBGA Pinout Table

Table 31: 280 LFBGA Pinout Table

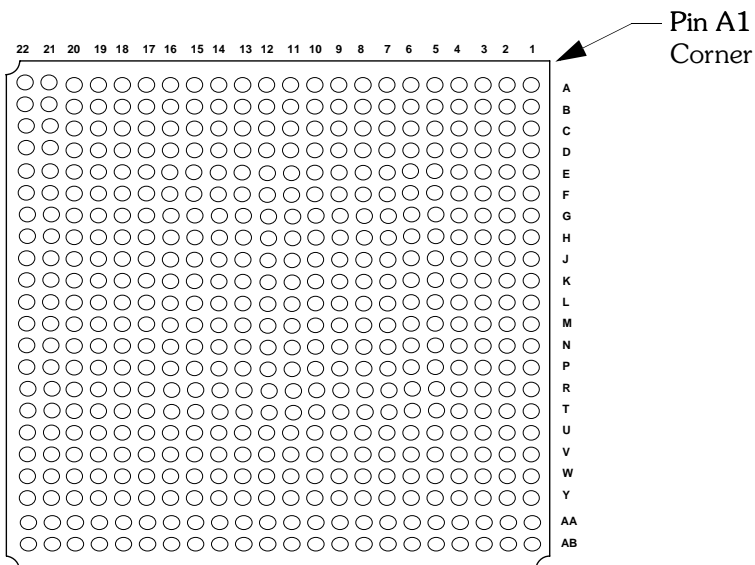
LFBGA	Function	LFBGA	Function	LFBGA	Function	LFBGA	Function	LFBGA	Function	LFBGA	Function
A1	PLLOUT(3)	C10	CLK(5)/ PLLIN(3)	E19	IOCTRL(D)	K16	I/O(C)	R4	I/O(H)	U13	I/O(B)
A2	GNDPLL(0)	C11	V _{CCIO} (E)	F1	INREF(G)	K17	I/O(D)	R5	GND	U14	IOCTRL(B)
A3	I/O(F)	C12	I/O(E)	F2	IOCTRL(G)	K18	I/O(C)	R6	GND	U15	V _{CCIO} (B)
A4	I/O(F)	C13	I/O(E)	F3	I/O(G)	K19	TRSTB	R7	V _{CC}	U16	I/O(B)
A5	I/O(F)	C14	I/O(E)	F4	I/O(G)	L1	I/O(H)	R8	V _{CC}	U17	TDO
A6	IOCTRL(F)	C15	V _{CCIO} (E)	F5	GND	L2	I/O(H)	R9	GND	U18	PLLST(2)
A7	I/O(F)	C16	I/O(E)	F15	V _{CC}	L3	V _{CCIO} (H)	R10	GND	U19	I/O(B)
A8	I/O(F)	C17	I/O(E)	F16	IOCTRL(D)	L4	I/O(H)	R11	V _{CC}	V1	PLLOUT(2)
A9	I/O(F)	C18	I/O(E)	F17	I/O(D)	L5	V _{CC}	R12	V _{CC}	V2	GNDPLL(3)
A10	CLK(7)	C19	I/O(E)	F18	I/O(D)	L15	GND	R13	V _{CC}	V3	GND
A11	I/O(E)	D1	I/O(G)	F19	I/O(D)	L16	I/O(C)	R14	V _{CC}	V4	I/O(A)
A12	I/O(E)	D2	I/O(G)	G1	I/O(G)	L17	V _{CCIO} (C)	R15	GND	V5	I/O(A)
A13	I/O(E)	D3	I/O(F)	G2	I/O(G)	L18	I/O(C)	R16	I/O(C)	V6	IOCTRL(A)
A14	IOCTRL(E)	D4	I/O(F)	G3	IOCTRL(G)	L19	I/O(C)	R17	V _{CCIO} (C)	V7	I/O(A)
A15	I/O(E)	D5	I/O(F)	G4	I/O(G)	M1	I/O(H)	R18	I/O(C)	V8	I/O(A)
A16	I/O(E)	D6	I/O(F)	G5	V _{CC}	M2	I/O(H)	R19	I/O(C)	V9	I/O(A)
A17	I/O(E)	D7	I/O(F)	G15	V _{CC}	M3	I/O(H)	T1	I/O(H)	V10	CLK(1)
A18	PLLST(1)	D8	I/O(F)	G16	I/O(D)	M4	I/O(H)	T2	I/O(H)	V11	CLK(4)/ DEDCLK/ PLLIN(0)
A19	GND	D9	CLK(8)	G17	I/O(D)	M5	V _{CC}	T3	I/O(A)	V12	I/O(B)
B1	PLLST(0)	D10	I/O(E)	G18	I/O(D)	M15	V _{CC}	T4	I/O(A)	V13	I/O(B)
B2	GND	D11	I/O(E)	G19	I/O(D)	M16	INREF(C)	T5	I/O(A)	V14	INREF(B)
B3	I/O(F)	D12	I/O(E)	H1	I/O(G)	M17	I/O(C)	T6	IOCTRL(A)	V15	I/O(B)
B4	I/O(F)	D13	INREF(E)	H2	I/O(G)	M18	I/O(C)	T7	I/O(A)	V16	I/O(B)
B5	I/O(F)	D14	I/O(E)	H3	I/O(G)	M19	I/O(C)	T8	I/O(A)	V17	I/O(B)
B6	INREF(F)	D15	I/O(E)	H4	I/O(G)	N1	IOCTRL(H)	T9	I/O(A)	V18	GNDPLL(2)
B7	I/O(F)	D16	I/O(D)	H5	V _{CC}	N2	I/O(H)	T10	I/O(A)	V19	GND
B8	I/O(F)	D17	I/O(D)	H15	V _{CC}	N3	I/O(H)	T11	CLK(3)/ PLLIN(1)	W1	GND
B9	TMS	D18	I/O(D)	H16	V _{CC}	N4	I/O(H)	T12	I/O(B)	W2	PLLST(3)
B10	CLK(6)	D19	I/O(D)	H17	I/O(D)	N5	V _{CC}	T13	I/O(B)	W3	I/O(A)
B11	I/O(E)	E1	I/O(G)	H18	I/O(D)	N15	V _{CC}	T14	I/O(B)	W4	I/O(A)
B12	I/O(E)	E2	I/O(G)	H19	I/O(D)	N16	I/O(C)	T15	I/O(B)	W5	I/O(A)
B13	IOCTRL(E)	E3	V _{CCIO} (G)	J1	I/O(G)	N17	I/O(C)	T16	I/O(B)	W6	I/O(A)
B14	I/O(E)	E4	I/O(F)	J2	I/O(G)	N18	IOCTRL(C)	T17	V _{CCPLL} (2)	W7	I/O(A)
B15	I/O(E)	E5	GND	J3	V _{CCIO} (G)	N19	IOCTRL(C)	T18	I/O(B)	W8	I/O(A)
B16	I/O(E)	E6	V _{CC}	J4	I/O(G)	P1	I/O(H)	T19	I/O(B)	W9	TDI
B17	V _{CCPLL} (1)	E7	V _{CC}	J5	GND	P2	I/O(H)	U1	I/O(A)	W10	CLK(2)/ PLLIN(2)
B18	GNDPLL(1)	E8	V _{CC}	J15	V _{CC}	P3	IOCTRL(H)	U2	I/O(A)	W11	I/O(B)
B19	PLLOUT(0)	E9	V _{CC}	J16	I/O(C)	P4	INREF(H)	U3	V _{CCPLL} (3)	W12	I/O(B)
C1	I/O(F)	E10	GND	J17	V _{CCIO} (D)	P5	V _{CC}	U4	I/O(A)	W13	I/O(B)
C2	V _{CCPLL} (0)	E11	GND	J18	I/O(D)	P15	GND	U5	V _{CCIO} (A)	W14	IOCTRL(B)
C3	I/O(F)	E12	V _{CC}	J19	I/O(D)	P16	I/O(C)	U6	INREF(A)	W15	I/O(B)
C4	I/O(F)	E13	V _{CC}	K1	V _{CC}	P17	I/O(C)	U7	I/O(A)	W16	I/O(B)
C5	V _{CCIO} (F)	E14	GND	K2	TCK	P18	I/O(C)	U8	I/O(A)	W17	I/O(B)
C6	IOCTRL(F)	E15	GND	K3	I/O(G)	P19	I/O(C)	U9	V _{CCIO} (A)	W18	I/O(B)
C7	I/O(F)	E16	I/O(D)	K4	I/O(G)	R1	I/O(H)	U10	CLK(0)	W19	PLLOUT(1)
C8	I/O(F)	E17	V _{CCIO} (D)	K5	GND	R2	I/O(H)	U11	V _{CCIO} (B)		
C9	V _{CCIO} (F)	E18	INREF(D)	K15	GND	R3	V _{CCIO} (H)	U12	I/O(B)		

QL7160 – 484 PBGA Pinout Diagram

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Bottom



QL7160 – 484 PBGA Pinout Table

Table 32: 484 PBGA Pinout Table

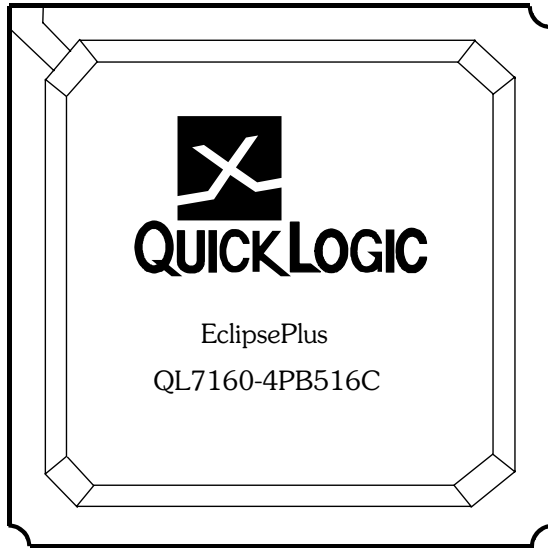
PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function
A1	I/O(A)	C1	I/O(A)	E1	IOCTRL(A)	G1	I/O(A)	J1	I/O(A)	L1	CLK(4)/ DEDCLK/ PLLIN(0)
A2	PLLIRST(3)	C2	I/O(A)	E2	I/O(A)	G2	I/O(A)	J2	I/O(A)	L2	CLK(0)
A3	I/O(A)	C3	V _{CCPLL} (3)	E3	I/O(A)	G3	I/O(A)	J3	I/O(A)	L3	CLK(2)/ PLLIN(2)
A4	I/O(A)	C4	PLLOUT(2)	E4	I/O(A)	G4	I/O(A)	J4	I/O(A)	L4	I/O(A)
A5	I/O(A)	C5	I/O(A)	E5	I/O(A)	G5	I/O(A)	J5	I/O(A)	L5	I/O(A)
A6	I/O(H)	C6	I/O(H)	E6	I/O(H)	G6	I/O(A)	J6	I/O(A)	L6	I/O(A)
A7	I/O(H)	C7	I/O(H)	E7	I/O(H)	G7	GND	J7	I/O(A)	L7	GND
A8	IOCTRL(H)	C8	I/O(H)	E8	I/O(H)	G8	I/O(H)	J8	V _{CC}	L8	GND
A9	I/O(H)	C9	IOCTRL(H)	E9	I/O(H)	G9	I/O(H)	J9	GND	L9	GND
A10	I/O(H)	C10	I/O(H)	E10	I/O(H)	G10	I/O(H)	J10	V _{CC}	L10	GND
A11	I/O(H)	C11	I/O(H)	E11	V _{CC}	G11	I/O(G)	J11	V _{CC}	L11	GND
A12	TCK	C12	I/O(H)	E12	I/O(G)	G12	GND	J12	GND	L12	GND
A13	I/O(G)	C13	I/O(G)	E13	I/O(G)	G13	I/O(G)	J13	V _{CC}	L13	GND
A14	I/O(G)	C14	I/O(G)	E14	I/O(G)	G14	I/O(G)	J14	GND	L14	V _{CC}
A15	I/O(G)	C15	I/O(G)	E15	IOCTRL(G)	G15	I/O(G)	J15	V _{CC}	L15	V _{CC}
A16	I/O(G)	C16	I/O(G)	E16	I/O(G)	G16	GND	J16	I/O(F)	L16	CLK(6)
A17	I/O(G)	C17	I/O(G)	E17	INREF(G)	G17	V _{CCIO} (F)	J17	V _{CCIO} (F)	L17	V _{CCIO} (F)
A18	I/O(G)	C18	I/O(G)	E18	I/O(G)	G18	I/O(F)	J18	I/O(F)	L18	I/O(F)
A19	I/O(F)	C19	I/O(F)	E19	I/O(F)	G19	I/O(F)	J19	I/O(F)	L19	CLK(8)
A20	GND	C20	GNDPLL(0)	E20	I/O(F)	G20	I/O(F)	J20	I/O(F)	L20	I/O(F)
A21	PLLOUT(3)	C21	I/O(F)	E21	I/O(F)	G21	INREF(F)	J21	I/O(F)	L21	I/O(F)
A22	I/O(F)	C22	I/O(F)	E22	I/O(F)	G22	I/O(F)	J22	I/O(F)	L22	I/O(F)
B1	I/O(A)	D1	I/O(A)	F1	I/O(A)	H1	I/O(A)	K1	TDI	M1	I/O(B)
B2	GND	D2	I/O(A)	F2	INREF(A)	H2	I/O(A)	K2	I/O(A)	M2	I/O(B)
B3	GNDPLL(3)	D3	I/O(A)	F3	I/O(A)	H3	I/O(A)	K3	I/O(A)	M3	I/O(B)
B4	GND	D4	I/O(A)	F4	I/O(A)	H4	I/O(A)	K4	I/O(A)	M4	CLK(3)/ PLLIN(1)
B5	I/O(A)	D5	I/O(A)	F5	I/O(A)	H5	IOCTRL(A)	K5	I/O(A)	M5	I/O(B)
B6	I/O(H)	D6	I/O(H)	F6	V _{CCIO} (A)	H6	V _{CCIO} (A)	K6	V _{CCIO} (A)	M6	V _{CCIO} (B)
B7	I/O(H)	D7	I/O(H)	F7	V _{CCIO} (H)	H7	I/O(H)	K7	I/O(A)	M7	CLK(1)
B8	INREF(H)	D8	I/O(H)	F8	I/O(H)	H8	GND	K8	V _{CC}	M8	V _{CC}
B9	I/O(H)	D9	I/O(H)	F9	V _{CCIO} (H)	H9	V _{CC}	K9	V _{CC}	M9	V _{CC}
B10	I/O(H)	D10	I/O(H)	F10	I/O(H)	H10	V _{CC}	K10	GND	M10	GND
B11	I/O(H)	D11	I/O(H)	F11	V _{CCIO} (H)	H11	V _{CC}	K11	GND	M11	GND
B12	I/O(G)	D12	I/O(G)	F12	V _{CCIO} (G)	H12	GND	K12	GND	M12	GND
B13	I/O(G)	D13	I/O(G)	F13	I/O(G)	H13	V _{CC}	K13	GND	M13	GND
B14	I/O(G)	D14	I/O(G)	F14	V _{CCIO} (G)	H14	V _{CC}	K14	V _{CC}	M14	GND
B15	I/O(G)	D15	IOCTRL(G)	F15	I/O(G)	H15	GND	K15	V _{CC}	M15	GND
B16	I/O(G)	D16	I/O(G)	F16	V _{CCIO} (G)	H16	I/O(F)	K16	I/O(F)	M16	GND
B17	I/O(G)	D17	I/O(G)	F17	I/O(G)	H17	I/O(F)	K17	I/O(F)	M17	I/O(E)
B18	I/O(G)	D18	I/O(F)	F18	I/O(F)	H18	I/O(F)	K18	I/O(F)	M18	I/O(E)
B19	PLLIRST(0)	D19	V _{CCPLL} (0)	F19	I/O(F)	H19	I/O(F)	K19	I/O(F)	M19	I/O(E)
B20	I/O(F)	D20	I/O(F)	F20	IOCTRL(F)	H20	I/O(F)	K20	I/O(F)	M20	CLK(7)
B21	I/O(F)	D21	I/O(F)	F21	I/O(F)	H21	I/O(F)	K21	I/O(F)	M21	CLK(5)/ PLLIN(3)
B22	I/O(F)	D22	I/O(F)	F22	IOCTRL(F)	H22	I/O(F)	K22	I/O(F)	M22	TMS

Table 32: 484 PBGA Pinout Table (Continued)

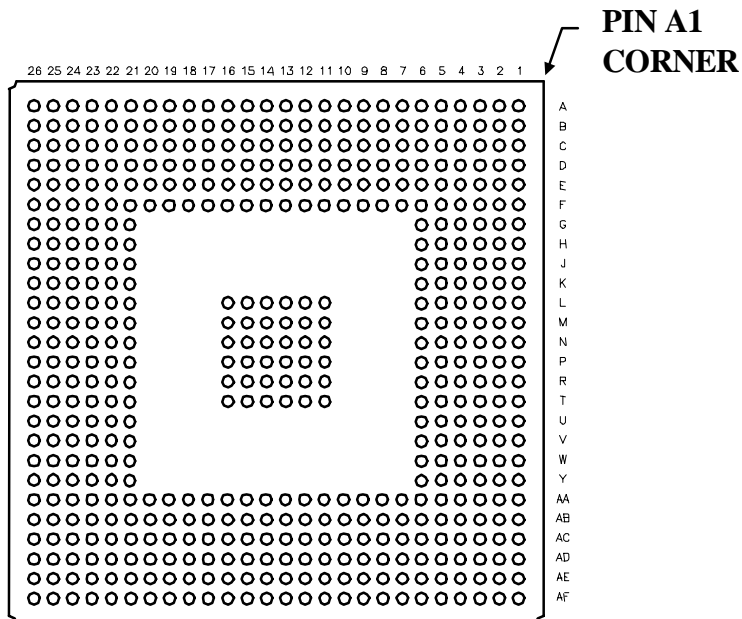
PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function
N1	I/O(B)	P16	I/O(E)	T9	I/O(C)	V2	I/O(B)	W17	I/O(D)	AA10	I/O(C)
N2	I/O(B)	P17	I/O(E)	T10	TRSTB	V3	I/O(B)	W18	I/O(E)	AA11	I/O(C)
N3	I/O(B)	P18	I/O(E)	T11	GND	V4	I/O(B)	W19	I/O(E)	AA12	I/O(D)
N4	I/O(B)	P19	I/O(E)	T12	I/O(C)	V5	I/O(B)	W20	I/O(E)	AA13	I/O(D)
N5	I/O(B)	P20	I/O(E)	T13	I/O(D)	V6	I/O(C)	W21	I/O(E)	AA14	I/O(D)
N6	I/O(B)	P21	I/O(E)	T14	I/O(D)	V7	I/O(C)	W22	I/O(E)	AA15	I/O(D)
N7	I/O(B)	P22	I/O(E)	T15	I/O(D)	V8	I/O(C)	Y1	I/O(B)	AA16	I/O(D)
N8	V _{CC}	R1	I/O(B)	T16	GND	V9	I/O(C)	Y2	I/O(B)	AA17	I/O(D)
N9	V _{CC}	R2	INREF(B)	T17	I/O(E)	V10	I/O(C)	Y3	V _{CCPLL(2)}	AA18	I/O(D)
N10	GND	R3	I/O(B)	T18	I/O(E)	V11	I/O(C)	Y4	I/O(C)	AA19	I/O(E)
N11	GND	R4	I/O(B)	T19	I/O(E)	V12	V _{CC}	Y5	I/O(C)	AA20	GNDPLL(1)
N12	GND	R5	I/O(B)	T20	I/O(E)	V13	I/O(D)	Y6	I/O(C)	AA21	I/O(E)
N13	GND	R6	I/O(B)	T21	IOCTRL(E)	V14	I/O(D)	Y7	I/O(C)	AA22	I/O(E)
N14	V _{CC}	R7	I/O(B)	T22	I/O(E)	V15	I/O(D)	Y8	IOCTRL(C)	AB1	I/O(B)
N15	V _{CC}	R8	GND	U1	IOCTRL(B)	V16	INREF(D)	Y9	I/O(C)	AB2	GNDPLL(2)
N16	I/O(E)	R9	V _{CC}	U2	I/O(B)	V17	I/O(D)	Y10	I/O(C)	AB3	PLLST(2)
N17	V _{CCIO(E)}	R10	V _{CC}	U3	IOCTRL(B)	V18	I/O(E)	Y11	I/O(D)	AB4	I/O(B)
N18	I/O(E)	R11	GND	U4	I/O(B)	V19	I/O(E)	Y12	I/O(D)	AB5	I/O(B)
N19	I/O(E)	R12	V _{CC}	U5	I/O(B)	V20	I/O(E)	Y13	I/O(D)	AB6	I/O(C)
N20	I/O(E)	R13	V _{CC}	U6	I/O(C)	V21	I/O(E)	Y14	I/O(D)	AB7	I/O(C)
N21	I/O(E)	R14	V _{CC}	U7	V _{CCIO(C)}	V22	I/O(E)	Y15	IOCTRL(D)	AB8	IOCTRL(C)
N22	I/O(E)	R15	GND	U8	I/O(C)	W1	I/O(B)	Y16	I/O(D)	AB9	I/O(C)
P1	I/O(B)	R16	I/O(D)	U9	V _{CCIO(C)}	W2	I/O(B)	Y17	I/O(D)	AB10	I/O(C)
P2	I/O(B)	R17	V _{CCIO(E)}	U10	I/O(C)	W3	I/O(B)	Y18	I/O(E)	AB11	I/O(C)
P3	I/O(B)	R18	I/O(E)	U11	V _{CCIO(C)}	W4	I/O(B)	Y19	PLLOUT(0)	AB12	I/O(D)
P4	I/O(B)	R19	I/O(E)	U12	V _{CCIO(D)}	W5	I/O(B)	Y20	PLLST(1)	AB13	I/O(D)
P5	I/O(B)	R20	I/O(E)	U13	I/O(D)	W6	I/O(C)	Y21	I/O(E)	AB14	I/O(D)
P6	V _{CCIO(B)}	R21	I/O(E)	U14	V _{CCIO(D)}	W7	I/O(C)	Y22	I/O(E)	AB15	I/O(D)
P7	I/O(B)	R22	I/O(E)	U15	I/O(D)	W8	I/O(C)	AA1	TDO	AB16	IOCTRL(D)
P8	V _{CC}	T1	I/O(B)	U16	V _{CCIO(D)}	W9	I/O(C)	AA2	PLLOUT(1)	AB17	I/O(D)
P9	GND	T2	I/O(B)	U17	V _{CCIO(E)}	W10	I/O(C)	AA3	GND	AB18	I/O(D)
P10	V _{CC}	T3	I/O(B)	U18	I/O(E)	W11	I/O(C)	AA4	I/O(B)	AB19	I/O(E)
P11	GND	T4	I/O(B)	U19	I/O(E)	W12	I/O(D)	AA5	I/O(C)	AB20	GND
P12	V _{CC}	T5	I/O(B)	U20	IOCTRL(E)	W13	I/O(D)	AA6	I/O(C)	AB21	V _{CCPLL(1)}
P13	V _{CC}	T6	V _{CCIO(B)}	U21	I/O(E)	W14	I/O(D)	AA7	I/O(C)	AB22	I/O(E)
P14	GND	T7	GND	U22	INREF(E)	W15	I/O(D)	AA8	INREF(C)		
P15	V _{CC}	T8	I/O(C)	V1	I/O(B)	W16	I/O(D)	AA9	I/O(C)		

QL7160 – 516 PBGA Pinout Diagram

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QL7160 – 516 PBGA Pinout Table

Table 33: 516 PBGA Pinout Table

PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function
A1	GND	B24	I/O(E)	D21	I/O(E)	F18	V _{CCIO} (E)	K5	I/O(G)	N6	GND
A2	I/O(F)	B25	I/O(E)	D22	I/O(E)	F19	V _{CC}	K6	GND	N11	GND
A3	I/O(F)	B26	PLLOUT(0)	D23	V _{CCPLL} (1)	F20	V _{CCIO} (E)	K21	GND	N12	GND
A4	I/O(F)	C1	I/O(F)	D24	I/O(E)	F21	GND	K22	I/O(D)	N13	GND
A5	I/O(F)	C2	I/O(F)	D25	I/O(E)	F22	I/O(E)	K23	I/O(D)	N14	GND
A6	I/O(F)	C3	I/O(F)	D26	I/O(D)	F23	I/O(D)	K24	I/O(D)	N15	GND
A7	IOCTRL(F)	C4	PLLOUT(3)	E1	I/O(G)	F24	I/O(D)	K25	I/O(D)	N16	GND
A8	I/O(F)	C5	I/O(F)	E2	I/O(G)	F25	I/O(D)	K26	I/O(D)	N21	GND
A9	I/O(F)	C6	I/O(F)	E3	I/O(G)	F26	I/O(D)	L1	I/O(G)	N22	I/O(D)
A10	I/O(F)	C7	I/O(F)	E4	V _{CCPLL} (0)	G1	I/O(G)	L2	I/O(G)	N23	I/O(D)
A11	I/O(F)	C8	INREF(F)	E5	I/O(F)	G2	INREF(G)	L3	I/O(G)	N24	I/O(D)
A12	I/O(F)	C9	I/O(F)	E6	I/O(F)	G3	I/O(G)	L4	I/O(G)	N25	I/O(D)
A13	I/O(E)	C10	I/O(F)	E7	I/O(F)	G4	I/O(G)	L5	V _{CC}	N26	I/O(D)
A14	I/O(E)	C11	I/O(F)	E8	V _{CC}	G5	I/O(G)	L6	V _{CC}	P1	I/O(H)
A15	I/O(E)	C12	I/O(F)	E9	I/O(F)	G6	V _{CCIO} (G)	L11	GND	P2	I/O(H)
A16	I/O(E)	C13	CLK(7)	E10	I/O(F)	G21	V _{CCIO} (D)	L12	GND	P3	I/O(H)
A17	I/O(E)	C14	I/O(E)	E11	I/O(F)	G22	I/O(D)	L13	GND	P4	V _{CC}
A18	IOCTRL(E)	C15	I/O(E)	E12	V _{CC}	G23	I/O(D)	L14	GND	P5	I/O(H)
A19	IOCTRL(E)	C16	I/O(E)	E13	I/O(F)	G24	I/O(D)	L15	GND	P6	V _{CCIO} (H)
A20	I/O(E)	C17	I/O(E)	E14	I/O(F)	G25	I/O(D)	L16	GND	P11	GND
A21	I/O(E)	C18	I/O(E)	E15	I/O(E)	G26	INREF(D)	L21	V _{CC}	P12	GND
A22	I/O(E)	C19	I/O(E)	E16	V _{CC}	H1	I/O(G)	L22	I/O(D)	P13	GND
A23	I/O(E)	C20	I/O(E)	E17	CLK(6)	H2	I/O(G)	L23	I/O(D)	P14	GND
A24	I/O(E)	C21	I/O(E)	E18	I/O(E)	H3	IOCTRL(G)	L24	I/O(D)	P15	GND
A25	PLLRST(1)	C22	I/O(E)	E19	I/O(E)	H4	I/O(G)	L25	I/O(D)	P16	GND
A26	GND	C23	I/O(E)	E20	I/O(E)	H5	I/O(G)	L26	I/O(D)	P21	V _{CCIO} (C)
B1	I/O(F)	C24	I/O(E)	E21	I/O(E)	H6	V _{CC}	M1	I/O(G)	P22	I/O(C)
B2	PLLRST(0)	C25	I/O(E)	E22	I/O(E)	H21	V _{CC}	M2	I/O(G)	P23	V _{CC}
B3	I/O(F)	C26	I/O(E)	E23	GNDPLL(1)	H22	V _{CC}	M3	I/O(G)	P24	I/O(C)
B4	I/O(F)	D1	I/O(G)	E24	I/O(E)	H23	I/O(D)	M4	I/O(G)	P25	I/O(C)
B5	I/O(F)	D2	I/O(G)	E25	I/O(D)	H24	IOCTRL(D)	M5	I/O(G)	P26	TRSTB
B6	I/O(F)	D3	I/O(F)	E26	I/O(D)	H25	IOCTRL(D)	M6	V _{CCIO} (G)	R1	I/O(H)
B7	IOCTRL(F)	D4	I/O(F)	F1	IOCTRL(G)	H26	I/O(D)	M11	GND	R2	I/O(H)
B8	I/O(F)	D5	GNDPLL(0)	F2	I/O(G)	J1	I/O(G)	M12	GND	R3	I/O(H)
B9	I/O(F)	D6	I/O(F)	F3	I/O(G)	J2	I/O(G)	M13	GND	R4	I/O(H)
B10	I/O(F)	D7	I/O(F)	F4	I/O(G)	J3	I/O(G)	M14	GND	R5	V _{CC}
B11	I/O(F)	D8	I/O(F)	F5	I/O(F)	J4	I/O(G)	M15	GND	R6	V _{CC}
B12	I/O(F)	D9	I/O(F)	F6	GND	J5	I/O(G)	M16	GND	R11	GND
B13	CLK(5)/ PLLIN(3)	D10	I/O(F)	F7	V _{CCIO} (F)	J6	V _{CCIO} (G)	M21	V _{CCIO} (D)	R12	GND
B14	I/O(E)	D11	I/O(F)	F8	V _{CC}	J21	V _{CCIO} (D)	M22	V _{CC}	R13	GND
B15	I/O(E)	D12	I/O(F)	F9	V _{CCIO} (F)	J22	I/O(D)	M23	I/O(D)	R14	GND
B16	I/O(E)	D13	TMS	F10	GND	J23	I/O(D)	M24	I/O(D)	R15	GND
B17	I/O(E)	D14	I/O(E)	F11	V _{CC}	J24	I/O(D)	M25	I/O(D)	R16	GND
B18	INREF(E)	D15	I/O(E)	F12	V _{CCIO} (F)	J25	I/O(D)	M26	I/O(D)	R21	V _{CC}
B19	I/O(E)	D16	I/O(F)	F13	GND	J26	I/O(D)	N1	TCK	R22	I/O(C)
B20	I/O(E)	D17	I/O(E)	F14	V _{CCIO} (E)	K1	I/O(G)	N2	I/O(H)	R23	I/O(C)
B21	I/O(E)	D18	I/O(F)	F15	V _{CC}	K2	I/O(G)	N3	I/O(G)	R24	I/O(C)
B22	I/O(E)	D19	CLK(8)	F16	V _{CC}	K3	I/O(G)	N4	I/O(G)	R25	I/O(C)
B23	I/O(E)	D20	I/O(E)	F17	GND	K4	I/O(G)	N5	I/O(G)	R26	I/O(C)

Table 33: 516 PBGA Pinout Table (Continued)

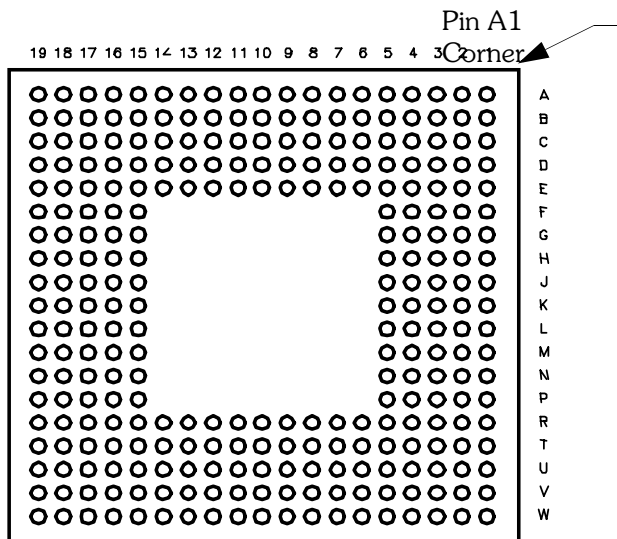
PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function
T1	I/O(H)	V22	I/O(C)	AA9	V _{CCIO(A)}	AB20	I/O(B)	AD5	I/O(A)	AE16	I/O(B)
T2	I/O(H)	V23	I/O(C)	AA10	GND	AB21	I/O(B)	AD6	I/O(A)	AE17	I/O(B)
T3	I/O(H)	V24	IOCTRL(C)	AA11	V _{CC}	AB22	GNDPLL(2)	AD7	I/O(A)	AE18	I/O(B)
T4	I/O(H)	V25	I/O(C)	AA12	V _{CCIO(A)}	AB23	I/O(B)	AD8	IOCTRL(A)	AE19	I/O(B)
T5	I/O(H)	V26	I/O(C)	AA13	GND	AB24	I/O(C)	AD9	I/O(A)	AE20	I/O(B)
T6	V _{CC}	W1	INREF(H)	AA14	V _{CCIO(B)}	AB25	I/O(C)	AD10	I/O(A)	AE21	I/O(B)
T11	GND	W2	I/O(H)	AA15	V _{CC}	AB26	I/O(C)	AD11	I/O(A)	AE22	I/O(B)
T12	GND	W3	I/O(H)	AA16	V _{CC}	AC1	I/O(A)	AD12	TDI	AE23	I/O(B)
T13	GND	W4	I/O(H)	AA17	GND	AC2	I/O(A)	AD13	CLK(4) DEDCLK/ PLLIN(0)	AE24	I/O(B)
T14	GND	W5	V _{CC}	AA18	V _{CCIO(B)}	AC3	I/O(A)	AD14	I/O(A)	AE25	PLLIRST(2)
T15	GND	W6	V _{CC}	AA19	V _{CC}	AC4	I/O(A)	AD15	I/O(B)	AE26	I/O(B)
T16	GND	W21	V _{CC}	AA20	V _{CCIO(B)}	AC5	I/O(A)	AD16	I/O(B)	AF1	I/O(A)
T21	V _{CC}	W22	I/O(C)	AA21	GND	AC6	I/O(A)	AD17	I/O(B)	AF2	I/O(A)
T22	V _{CC}	W23	I/O(C)	AA22	V _{CCPLL(2)}	AC7	I/O(A)	AD18	INREF(B)	AF3	I/O(A)
T23	I/O(C)	W24	I/O(C)	AA23	I/O(C)	AC8	I/O(A)	AD19	I/O(B)	AF4	I/O(A)
T24	I/O(C)	W25	INREF(C)	AA24	I/O(C)	AC9	I/O(A)	AD20	I/O(B)	AF5	I/O(A)
T25	I/O(C)	W26	I/O(C)	AA25	I/O(C)	AC10	I/O(A)	AD21	I/O(B)	AF6	IOCTRL(A)
T26	I/O(C)	Y1	I/O(H)	AA26	I/O(C)	AC11	I/O(A)	AD22	I/O(B)	AF7	I/O(A)
U1	I/O(H)	Y2	I/O(H)	AB1	I/O(H)	AC12	I/O(A)	AD23	I/O(B)	AF8	I/O(A)
U2	I/O(H)	Y3	I/O(H)	AB2	I/O(H)	AC13	I/O(A)	AD24	GND	AF9	I/O(A)
U3	I/O(H)	Y4	I/O(H)	AB3	I/O(A)	AC14	CLK(1)	AD25	I/O(B)	AF10	I/O(A)
U4	I/O(H)	Y5	I/O(H)	AB4	GNDPLL(3)	AC15	I/O(B)	AD26	I/O(B)	AF11	I/O(A)
U5	I/O(H)	Y6	V _{CCIO(H)}	AB5	V _{CCPLL(3)}	AC16	I/O(B)	AE1	GND	AF12	CLK(2)/P LLIN(2)
U6	GND	Y21	V _{CCIO(C)}	AB6	I/O(A)	AC17	I/O(B)	AE2	GND	AF13	I/O(B)
U21	GND	Y22	I/O(C)	AB7	I/O(A)	AC18	I/O(B)	AE3	I/O(A)	AF14	I/O(B)
U22	I/O(C)	Y23	I/O(C)	AB8	I/O(A)	AC19	I/O(B)	AE4	I/O(A)	AF15	I/O(B)
U23	I/O(C)	Y24	I/O(C)	AB9	I/O(A)	AC20	I/O(B)	AE5	I/O(A)	AF16	I/O(B)
U24	I/O(C)	Y25	I/O(C)	AB10	I/O(A)	AC21	I/O(B)	AE6	I/O(A)	AF17	I/O(B)
U25	I/O(C)	Y26	IOCTRL(C)	AB11	V _{CC}	AC22	TDO	AE7	INREF(A)	AF18	I/O(B)
U26	I/O(C)	AA1	I/O(H)	AB12	I/O(A)	AC23	PLLOUT(1)	AE8	I/O(A)	AF19	IOCTRL(B)
V1	I/O(H)	AA2	I/O(H)	AB13	I/O(A)	AC24	I/O(B)	AE9	I/O(A)	AF20	IOCTRL(B)
V2	IOCTRL(H)	AA3	I/O(H)	AB14	CLK(3)/ PLLIN(1)	AC25	I/O(B)	AE10	I/O(A)	AF21	I/O(B)
V3	IOCTRL(H)	AA4	I/O(A)	AB15	V _{CC}	AC26	I/O(C)	AE11	I/O(A)	AF22	I/O(B)
V4	I/O(H)	AA5	I/O(A)	AB16	I/O(B)	AD1	I/O(A)	AE12	CLK(0)	AF23	I/O(B)
V5	I/O(H)	AA6	GND	AB17	I/O(B)	AD2	PLLOUT(2)	AE13	I/O(B)	AF24	I/O(B)
V6	V _{CCIO(H)}	AA7	V _{CCIO(A)}	AB18	I/O(B)	AD3	PLLIRST(3)	AE14	I/O(B)	AF25	I/O(B)
V21	V _{CCIO(C)}	AA8	V _{CC}	AB19	V _{CC}	AD4	I/O(A)	AE15	I/O(B)	AF26	I/O(B)

QL7180 – 280 LFBGA Pinout Diagram

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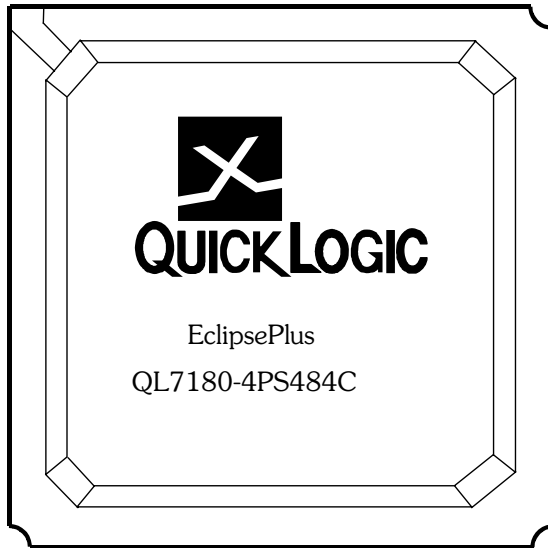
QL7180 – 280 LFBGA Pinout Table

Table 34: 280 LFBGA Pinout Table

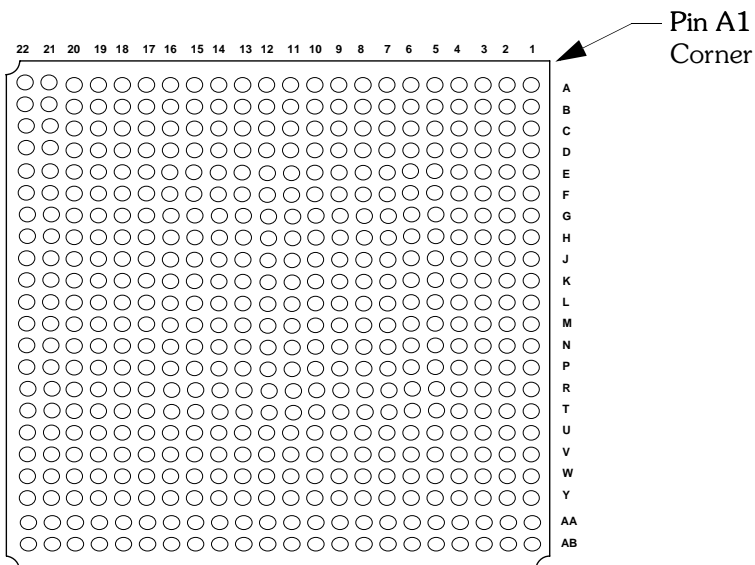
LFBGA	Function	LFBGA	Function	LFBGA	Function	LFBGA	Function	LFBGA	Function	LFBGA	Function
A1	PLL0UT(3)	C10	CLK(5)/ PLLIN(3)	E19	IOCTRL(D)	K16	I/O(C)	R4	I/O(H)	U13	I/O(B)
A2	GNDPLL(0)	C11	V _{CCIO} (E)	F1	INREF(G)	K17	I/O(D)	R5	GND	U14	IOCTRL(B)
A3	I/O(F)	C12	I/O(E)	F2	IOCTRL(G)	K18	I/O(C)	R6	GND	U15	V _{CCIO} (B)
A4	I/O(F)	C13	I/O(E)	F3	I/O(G)	K19	TRSTB	R7	V _{CC}	U16	I/O(B)
A5	I/O(F)	C14	I/O(E)	F4	I/O(G)	L1	I/O(H)	R8	V _{CC}	U17	TDO
A6	IOCTRL(F)	C15	V _{CCIO} (E)	F5	GND	L2	I/O(H)	R9	GND	U18	PLLST(2)
A7	I/O(F)	C16	I/O(E)	F15	V _{CC}	L3	V _{CCIO} (H)	R10	GND	U19	I/O(B)
A8	I/O(F)	C17	I/O(E)	F16	IOCTRL(D)	L4	I/O(H)	R11	V _{CC}	V1	PLL0UT(2)
A9	I/O(F)	C18	I/O(E)	F17	I/O(D)	L5	V _{CC}	R12	V _{CC}	V2	GNDPLL(3)
A10	CLK(7)	C19	I/O(E)	F18	I/O(D)	L15	GND	R13	V _{CC}	V3	GND
A11	I/O(E)	D1	I/O(G)	F19	I/O(D)	L16	I/O(C)	R14	V _{CC}	V4	I/O(A)
A12	I/O(E)	D2	I/O(G)	G1	I/O(G)	L17	V _{CCIO} (C)	R15	GND	V5	I/O(A)
A13	I/O(E)	D3	I/O(F)	G2	I/O(G)	L18	I/O(C)	R16	I/O(C)	V6	IOCTRL(A)
A14	IOCTRL(E)	D4	I/O(F)	G3	IOCTRL(G)	L19	I/O(C)	R17	V _{CCIO} (C)	V7	I/O(A)
A15	I/O(E)	D5	I/O(F)	G4	I/O(G)	M1	I/O(H)	R18	I/O(C)	V8	I/O(A)
A16	I/O(E)	D6	I/O(F)	G5	V _{CC}	M2	I/O(H)	R19	I/O(C)	V9	I/O(A)
A17	I/O(E)	D7	I/O(F)	G15	V _{CC}	M3	I/O(H)	T1	I/O(H)	V10	CLK(1)
A18	PLLST(1)	D8	I/O(F)	G16	I/O(D)	M4	I/O(H)	T2	I/O(H)	V11	CLK(4)/ DEDCLK/ PLLIN(0)
A19	GND	D9	CLK(8)	G17	I/O(D)	M5	V _{CC}	T3	I/O(A)	V12	I/O(B)
B1	PLLST(0)	D10	I/O(E)	G18	I/O(D)	M15	V _{CC}	T4	I/O(A)	V13	I/O(B)
B2	GND	D11	I/O(E)	G19	I/O(D)	M16	INREF(C)	T5	I/O(A)	V14	INREF(B)
B3	I/O(F)	D12	I/O(E)	H1	I/O(G)	M17	I/O(C)	T6	IOCTRL(A)	V15	I/O(B)
B4	I/O(F)	D13	INREF(E)	H2	I/O(G)	M18	I/O(C)	T7	I/O(A)	V16	I/O(B)
B5	I/O(F)	D14	I/O(E)	H3	I/O(G)	M19	I/O(C)	T8	I/O(A)	V17	I/O(B)
B6	INREF(F)	D15	I/O(E)	H4	I/O(G)	N1	IOCTRL(H)	T9	I/O(A)	V18	GNDPLL(2)
B7	I/O(F)	D16	I/O(D)	H5	V _{CC}	N2	I/O(H)	T10	I/O(A)	V19	GND
B8	I/O(F)	D17	I/O(D)	H15	V _{CC}	N3	I/O(H)	T11	CLK(3)/ PLLIN(1)	W1	GND
B9	TMS	D18	I/O(D)	H16	V _{CC}	N4	I/O(H)	T12	I/O(B)	W2	PLLST(3)
B10	CLK(6)	D19	I/O(D)	H17	I/O(D)	N5	V _{CC}	T13	I/O(B)	W3	I/O(A)
B11	I/O(E)	E1	I/O(G)	H18	I/O(D)	N15	V _{CC}	T14	I/O(B)	W4	I/O(A)
B12	I/O(E)	E2	I/O(G)	H19	I/O(D)	N16	I/O(C)	T15	I/O(B)	W5	I/O(A)
B13	IOCTRL(E)	E3	V _{CCIO} (G)	J1	I/O(G)	N17	I/O(C)	T16	I/O(B)	W6	I/O(A)
B14	I/O(E)	E4	I/O(F)	J2	I/O(G)	N18	IOCTRL(C)	T17	V _{CC} PLL(2)	W7	I/O(A)
B15	I/O(E)	E5	GND	J3	V _{CCIO} (G)	N19	IOCTRL(C)	T18	I/O(B)	W8	I/O(A)
B16	I/O(E)	E6	V _{CC}	J4	I/O(G)	P1	I/O(H)	T19	I/O(B)	W9	TDI
B17	V _{CC} PLL(1)	E7	V _{CC}	J5	GND	P2	I/O(H)	U1	I/O(A)	W10	CLK(2)/ PLLIN(2)
B18	GNDPLL(1)	E8	V _{CC}	J15	V _{CC}	P3	IOCTRL(H)	U2	I/O(A)	W11	I/O(B)
B19	PLL0UT(0)	E9	V _{CC}	J16	I/O(C)	P4	INREF(H)	U3	V _{CC} PLL(3)	W12	I/O(B)
C1	I/O(F)	E10	GND	J17	V _{CCIO} (D)	P5	V _{CC}	U4	I/O(A)	W13	I/O(B)
C2	V _{CC} PLL(0)	E11	GND	J18	I/O(D)	P15	GND	U5	V _{CCIO} (A)	W14	IOCTRL(B)
C3	I/O(F)	E12	V _{CC}	J19	I/O(D)	P16	I/O(C)	U6	INREF(A)	W15	I/O(B)
C4	I/O(F)	E13	V _{CC}	K1	V _{CC}	P17	I/O(C)	U7	I/O(A)	W16	I/O(B)
C5	V _{CCIO} (F)	E14	GND	K2	TCK	P18	I/O(C)	U8	I/O(A)	W17	I/O(B)
C6	IOCTRL(F)	E15	GND	K3	I/O(G)	P19	I/O(C)	U9	V _{CCIO} (A)	W18	I/O(B)
C7	I/O(F)	E16	I/O(D)	K4	I/O(G)	R1	I/O(H)	U10	CLK(0)	W19	PLL0UT(1)
C8	I/O(F)	E17	V _{CCIO} (D)	K5	GND	R2	I/O(H)	U11	V _{CCIO} (B)		
C9	V _{CCIO} (F)	E18	INREF(D)	K15	GND	R3	V _{CCIO} (H)	U12	I/O(B)		

QL7180 – 484 PBGA Pinout Diagram

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Bottom



QL7180 – 484 PBGA Pinout Table

Table 35: 484 PBGA Pinout Table

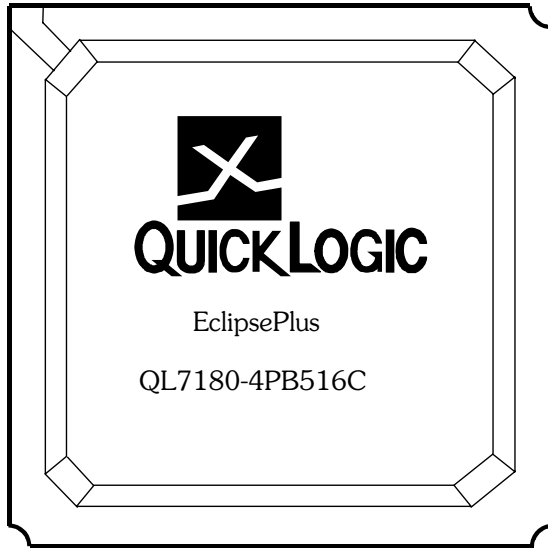
PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function
A1	I/O(A)	C1	I/O(A)	E1	IOCTRL(A)	G1	I/O(A)	J1	I/O(A)	L1	CLK(4) DEDCLK/ PLLIN(0)
A2	PLLRST(3)	C2	I/O(A)	E2	I/O(A)	G2	I/O(A)	J2	I/O(A)	L2	CLK(0)
A3	I/O(A)	C3	V _{CC} PLL(3)	E3	I/O(A)	G3	I/O(A)	J3	I/O(A)	L3	CLK(2)/PLLIN(2)
A4	I/O(A)	C4	PLLOUT(2)	E4	I/O(A)	G4	I/O(A)	J4	I/O(A)	L4	I/O(A)
A5	I/O(A)	C5	I/O(A)	E5	I/O(A)	G5	I/O(A)	J5	I/O(A)	L5	I/O(A)
A6	I/O(H)	C6	I/O(H)	E6	I/O(H)	G6	I/O(A)	J6	I/O(A)	L6	I/O(A)
A7	I/O(H)	C7	I/O(H)	E7	I/O(H)	G7	GND	J7	I/O(A)	L7	GND
A8	IOCTRL(H)	C8	I/O(H)	E8	I/O(H)	G8	I/O(H)	J8	V _{CC}	L8	GND
A9	I/O(H)	C9	IOCTRL(H)	E9	I/O(H)	G9	I/O(H)	J9	GND	L9	GND
A10	I/O(H)	C10	I/O(H)	E10	I/O(H)	G10	I/O(H)	J10	V _{CC}	L10	GND
A11	I/O(H)	C11	I/O(H)	E11	V _{CC}	G11	I/O(G)	J11	V _{CC}	L11	GND
A12	TCK	C12	I/O(H)	E12	I/O(G)	G12	GND	J12	GND	L12	GND
A13	I/O(G)	C13	I/O(G)	E13	I/O(G)	G13	I/O(G)	J13	V _{CC}	L13	GND
A14	I/O(G)	C14	I/O(G)	E14	I/O(G)	G14	I/O(G)	J14	GND	L14	V _{CC}
A15	I/O(G)	C15	I/O(G)	E15	IOCTRL(G)	G15	I/O(G)	J15	V _{CC}	L15	V _{CC}
A16	I/O(G)	C16	I/O(G)	E16	I/O(G)	G16	GND	J16	I/O(F)	L16	CLK(6)
A17	I/O(G)	C17	I/O(G)	E17	INREF(G)	G17	V _{CCIO} (F)	J17	V _{CCIO} (F)	L17	V _{CCIO} (F)
A18	I/O(G)	C18	I/O(G)	E18	I/O(G)	G18	I/O(F)	J18	I/O(F)	L18	I/O(F)
A19	I/O(F)	C19	I/O(F)	E19	I/O(F)	G19	I/O(F)	J19	I/O(F)	L19	CLK(8)
A20	GND	C20	GNDPLL(0)	E20	I/O(F)	G20	I/O(F)	J20	I/O(F)	L20	I/O(F)
A21	PLLOUT(3)	C21	I/O(F)	E21	I/O(F)	G21	INREF(F)	J21	I/O(F)	L21	I/O(F)
A22	I/O(F)	C22	I/O(F)	E22	I/O(F)	G22	I/O(F)	J22	I/O(F)	L22	I/O(F)
B1	I/O(A)	D1	I/O(A)	F1	I/O(A)	H1	I/O(A)	K1	TDI	M1	I/O(B)
B2	GND	D2	I/O(A)	F2	INREF(A)	H2	I/O(A)	K2	I/O(A)	M2	I/O(B)
B3	GNDPLL(3)	D3	I/O(A)	F3	I/O(A)	H3	I/O(A)	K3	I/O(A)	M3	I/O(B)
B4	GND	D4	I/O(A)	F4	I/O(A)	H4	I/O(A)	K4	I/O(A)	M4	CLK(3)/PLLIN(1)
B5	I/O(A)	D5	I/O(A)	F5	I/O(A)	H5	IOCTRL(A)	K5	I/O(A)	M5	I/O(B)
B6	I/O(H)	D6	I/O(H)	F6	V _{CCIO} (A)	H6	V _{CCIO} (A)	K6	V _{CCIO} (A)	M6	V _{CCIO} (B)
B7	I/O(H)	D7	I/O(H)	F7	V _{CCIO} (H)	H7	I/O(H)	K7	I/O(A)	M7	CLK(1)
B8	INREF(H)	D8	I/O(H)	F8	I/O(H)	H8	GND	K8	V _{CC}	M8	V _{CC}
B9	I/O(H)	D9	I/O(H)	F9	V _{CCIO} (H)	H9	V _{CC}	K9	V _{CC}	M9	V _{CC}
B10	I/O(H)	D10	I/O(H)	F10	I/O(H)	H10	V _{CC}	K10	GND	M10	GND
B11	I/O(H)	D11	I/O(H)	F11	V _{CCIO} (H)	H11	V _{CC}	K11	GND	M11	GND
B12	I/O(G)	D12	I/O(G)	F12	V _{CCIO} (G)	H12	GND	K12	GND	M12	GND
B13	I/O(G)	D13	I/O(G)	F13	I/O(G)	H13	V _{CC}	K13	GND	M13	GND
B14	I/O(G)	D14	I/O(G)	F14	V _{CCIO} (G)	H14	V _{CC}	K14	V _{CC}	M14	GND
B15	I/O(G)	D15	IOCTRL(G)	F15	I/O(G)	H15	GND	K15	V _{CC}	M15	GND
B16	I/O(G)	D16	I/O(G)	F16	V _{CCIO} (G)	H16	I/O(F)	K16	I/O(F)	M16	GND
B17	I/O(G)	D17	I/O(G)	F17	I/O(G)	H17	I/O(F)	K17	I/O(F)	M17	I/O(E)
B18	I/O(G)	D18	I/O(F)	F18	I/O(F)	H18	I/O(F)	K18	I/O(F)	M18	I/O(E)
B19	PLLRST(0)	D19	V _{CC} PLL(0)	F19	I/O(F)	H19	I/O(F)	K19	I/O(F)	M19	I/O(E)
B20	I/O(F)	D20	I/O(F)	F20	IOCTRL(F)	H20	I/O(F)	K20	I/O(F)	M20	CLK(7)
B21	I/O(F)	D21	I/O(F)	F21	I/O(F)	H21	I/O(F)	K21	I/O(F)	M21	CLK(5)/PLLIN(3)
B22	I/O(F)	D22	I/O(F)	F22	IOCTRL(F)	H22	I/O(F)	K22	I/O(F)	M22	TMS

Table 35: 484 PBGA Pinout Table (Continued)

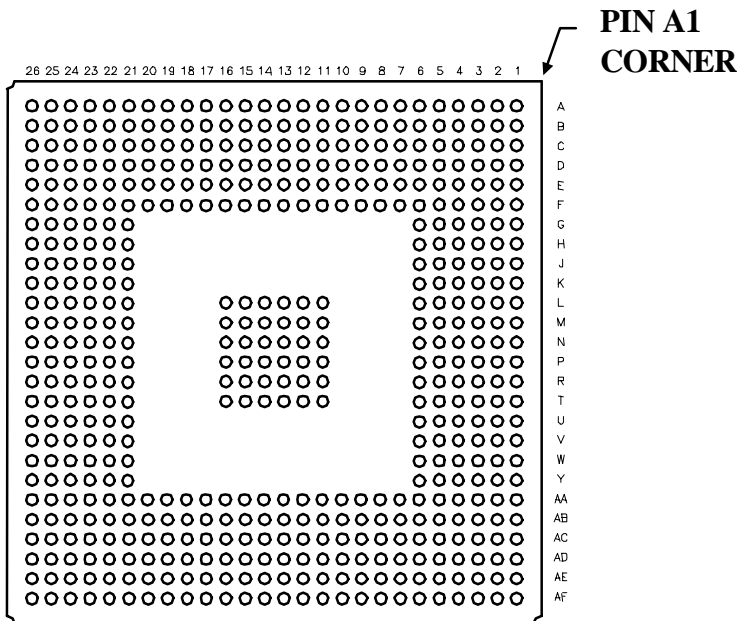
PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function
N1	I/O(B)	P16	I/O(E)	T9	I/O(C)	V2	I/O(B)	W17	I/O(D)	AA10	I/O(C)
N2	I/O(B)	P17	I/O(E)	T10	TRSTB	V3	I/O(B)	W18	I/O(E)	AA11	I/O(C)
N3	I/O(B)	P18	I/O(E)	T11	GND	V4	I/O(B)	W19	I/O(E)	AA12	I/O(D)
N4	I/O(B)	P19	I/O(E)	T12	I/O(C)	V5	I/O(B)	W20	I/O(E)	AA13	I/O(D)
N5	I/O(B)	P20	I/O(E)	T13	I/O(D)	V6	I/O(C)	W21	I/O(E)	AA14	I/O(D)
N6	I/O(B)	P21	I/O(E)	T14	I/O(D)	V7	I/O(C)	W22	I/O(E)	AA15	I/O(D)
N7	I/O(B)	P22	I/O(E)	T15	I/O(D)	V8	I/O(C)	Y1	I/O(B)	AA16	I/O(D)
N8	V _{CC}	R1	I/O(B)	T16	GND	V9	I/O(C)	Y2	I/O(B)	AA17	I/O(D)
N9	V _{CC}	R2	INREF(B)	T17	I/O(E)	V10	I/O(C)	Y3	V _{CC} PLL(2)	AA18	I/O(D)
N10	GND	R3	I/O(B)	T18	I/O(E)	V11	I/O(C)	Y4	I/O(C)	AA19	I/O(E)
N11	GND	R4	I/O(B)	T19	I/O(E)	V12	V _{CC}	Y5	I/O(C)	AA20	GNDPLL(1)
N12	GND	R5	I/O(B)	T20	I/O(E)	V13	I/O(D)	Y6	I/O(C)	AA21	I/O(E)
N13	GND	R6	I/O(B)	T21	IOCTRL(E)	V14	I/O(D)	Y7	I/O(C)	AA22	I/O(E)
N14	V _{CC}	R7	I/O(B)	T22	I/O(E)	V15	I/O(D)	Y8	IOCTRL(C)	AB1	I/O(B)
N15	V _{CC}	R8	GND	U1	IOCTRL(B)	V16	INREF(D)	Y9	I/O(C)	AB2	GNDPLL(2)
N16	I/O(E)	R9	V _{CC}	U2	I/O(B)	V17	I/O(D)	Y10	I/O(C)	AB3	PLL RST(2)
N17	V _{CCIO} (E)	R10	V _{CC}	U3	IOCTRL(B)	V18	I/O(E)	Y11	I/O(D)	AB4	I/O(B)
N18	I/O(E)	R11	GND	U4	I/O(B)	V19	I/O(E)	Y12	I/O(D)	AB5	I/O(B)
N19	I/O(E)	R12	V _{CC}	U5	I/O(B)	V20	I/O(E)	Y13	I/O(D)	AB6	I/O(C)
N20	I/O(E)	R13	V _{CC}	U6	I/O(C)	V21	I/O(E)	Y14	I/O(D)	AB7	I/O(C)
N21	I/O(E)	R14	V _{CC}	U7	V _{CCIO} (C)	V22	I/O(E)	Y15	IOCTRL(D)	AB8	IOCTRL(C)
N22	I/O(E)	R15	GND	U8	I/O(C)	W1	I/O(B)	Y16	I/O(D)	AB9	I/O(C)
P1	I/O(B)	R16	I/O(D)	U9	V _{CCIO} (C)	W2	I/O(B)	Y17	I/O(D)	AB10	I/O(C)
P2	I/O(B)	R17	V _{CCIO} (E)	U10	I/O(C)	W3	I/O(B)	Y18	I/O(E)	AB11	I/O(C)
P3	I/O(B)	R18	I/O(E)	U11	V _{CCIO} (C)	W4	I/O(B)	Y19	PLLOUT(0)	AB12	I/O(D)
P4	I/O(B)	R19	I/O(E)	U12	V _{CCIO} (D)	W5	I/O(B)	Y20	PLL RST(1)	AB13	I/O(D)
P5	I/O(B)	R20	I/O(E)	U13	I/O(D)	W6	I/O(C)	Y21	I/O(E)	AB14	I/O(D)
P6	V _{CCIO} (B)	R21	I/O(E)	U14	V _{CCIO} (D)	W7	I/O(C)	Y22	I/O(E)	AB15	I/O(D)
P7	I/O(B)	R22	I/O(E)	U15	I/O(D)	W8	I/O(C)	AA1	TDO	AB16	IOCTRL(D)
P8	V _{CC}	T1	I/O(B)	U16	V _{CCIO} (D)	W9	I/O(C)	AA2	PLLOUT(1)	AB17	I/O(D)
P9	GND	T2	I/O(B)	U17	V _{CCIO} (E)	W10	I/O(C)	AA3	GND	AB18	I/O(D)
P10	V _{CC}	T3	I/O(B)	U18	I/O(E)	W11	I/O(C)	AA4	I/O(B)	AB19	I/O(E)
P11	GND	T4	I/O(B)	U19	I/O(E)	W12	I/O(D)	AA5	I/O(C)	AB20	GND
P12	V _{CC}	T5	I/O(B)	U20	IOCTRL(E)	W13	I/O(D)	AA6	I/O(C)	AB21	V _{CC} PLL(1)
P13	V _{CC}	T6	V _{CCIO} (B)	U21	I/O(E)	W14	I/O(D)	AA7	I/O(C)	AB22	I/O(E)
P14	GND	T7	GND	U22	INREF(E)	W15	I/O(D)	AA8	INREF(C)		
P15	V _{CC}	T8	I/O(C)	V1	I/O(B)	W16	I/O(D)	AA9	I/O(C)		

QL7180 – 516 PBGA Pinout Diagram

Top



Bottom



QL7180 – 516 PBGA Pinout Table

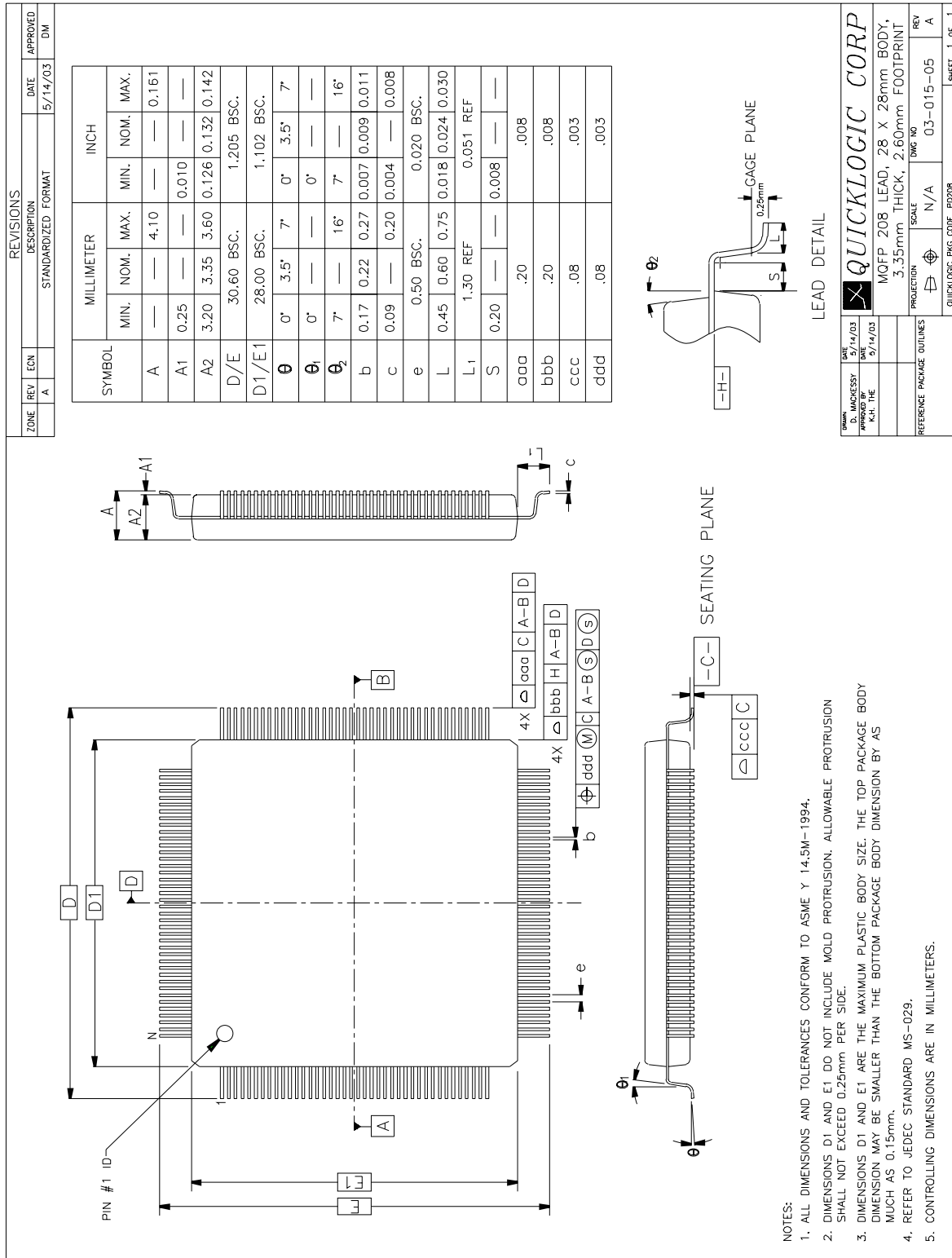
Table 36: 516 PBGA Pinout Table

PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function
A1	GND	B24	I/O(E)	D21	I/O(E)	F18	V _{CCIO} (E)	K5	I/O(G)	N6	GND
A2	I/O(F)	B25	I/O(E)	D22	I/O(E)	F19	V _{CC}	K6	GND	N11	GND
A3	I/O(F)	B26	PLLOUT(0)	D23	V _{CC} PLL(1)	F20	V _{CCIO} (E)	K21	GND	N12	GND
A4	I/O(F)	C1	I/O(F)	D24	I/O(E)	F21	GND	K22	I/O(D)	N13	GND
A5	I/O(F)	C2	I/O(F)	D25	I/O(E)	F22	I/O(E)	K23	I/O(D)	N14	GND
A6	I/O(F)	C3	I/O(F)	D26	I/O(D)	F23	I/O(D)	K24	I/O(D)	N15	GND
A7	IOCTRL(F)	C4	PLLOUT(3)	E1	I/O(G)	F24	I/O(D)	K25	I/O(D)	N16	GND
A8	I/O(F)	C5	I/O(F)	E2	I/O(G)	F25	I/O(D)	K26	I/O(D)	N21	GND
A9	I/O(F)	C6	I/O(F)	E3	I/O(G)	F26	I/O(D)	L1	I/O(G)	N22	I/O(D)
A10	I/O(F)	C7	I/O(F)	E4	V _{CC} PLL(0)	G1	I/O(G)	L2	I/O(G)	N23	I/O(D)
A11	I/O(F)	C8	INREF(F)	E5	I/O(F)	G2	INREF(G)	L3	I/O(G)	N24	I/O(D)
A12	I/O(F)	C9	I/O(F)	E6	I/O(F)	G3	I/O(G)	L4	I/O(G)	N25	I/O(D)
A13	I/O(E)	C10	I/O(F)	E7	I/O(F)	G4	I/O(G)	L5	V _{CC}	N26	I/O(D)
A14	I/O(E)	C11	I/O(F)	E8	V _{CC}	G5	I/O(G)	L6	V _{CC}	P1	I/O(H)
A15	I/O(E)	C12	I/O(F)	E9	I/O(F)	G6	V _{CCIO} (G)	L11	GND	P2	I/O(H)
A16	I/O(E)	C13	CLK(7)	E10	I/O(F)	G21	V _{CCIO} (D)	L12	GND	P3	I/O(H)
A17	I/O(E)	C14	I/O(E)	E11	I/O(F)	G22	I/O(D)	L13	GND	P4	V _{CC}
A18	IOCTRL(E)	C15	I/O(E)	E12	V _{CC}	G23	I/O(D)	L14	GND	P5	I/O(H)
A19	IOCTRL(E)	C16	I/O(E)	E13	I/O(F)	G24	I/O(D)	L15	GND	P6	V _{CCIO} (H)
A20	I/O(E)	C17	I/O(E)	E14	I/O(F)	G25	I/O(D)	L16	GND	P11	GND
A21	I/O(E)	C18	I/O(E)	E15	I/O(E)	G26	INREF(D)	L21	V _{CC}	P12	GND
A22	I/O(E)	C19	I/O(E)	E16	V _{CC}	H1	I/O(G)	L22	I/O(D)	P13	GND
A23	I/O(E)	C20	I/O(E)	E17	CLK(6)	H2	I/O(G)	L23	I/O(D)	P14	GND
A24	I/O(E)	C21	I/O(E)	E18	I/O(E)	H3	IOCTRL(G)	L24	I/O(D)	P15	GND
A25	PLLST(1)	C22	I/O(E)	E19	I/O(E)	H4	I/O(G)	L25	I/O(D)	P16	GND
A26	GND	C23	I/O(E)	E20	I/O(E)	H5	I/O(G)	L26	I/O(D)	P21	V _{CCIO} (C)
B1	I/O(F)	C24	I/O(E)	E21	I/O(E)	H6	V _{CC}	M1	I/O(G)	P22	I/O(C)
B2	PLLST(0)	C25	I/O(E)	E22	I/O(E)	H21	V _{CC}	M2	I/O(G)	P23	V _{CC}
B3	I/O(F)	C26	I/O(E)	E23	GNDPLL(1)	H22	V _{CC}	M3	I/O(G)	P24	I/O(C)
B4	I/O(F)	D1	I/O(G)	E24	I/O(E)	H23	I/O(D)	M4	I/O(G)	P25	I/O(C)
B5	I/O(F)	D2	I/O(G)	E25	I/O(D)	H24	IOCTRL(D)	M5	I/O(G)	P26	TRSTB
B6	I/O(F)	D3	I/O(F)	E26	I/O(D)	H25	IOCTRL(D)	M6	V _{CCIO} (G)	R1	I/O(H)
B7	IOCTRL(F)	D4	I/O(F)	F1	IOCTRL(G)	H26	I/O(D)	M11	GND	R2	I/O(H)
B8	I/O(F)	D5	GNDPLL(0)	F2	I/O(G)	J1	I/O(G)	M12	GND	R3	I/O(H)
B9	I/O(F)	D6	I/O(F)	F3	I/O(G)	J2	I/O(G)	M13	GND	R4	I/O(H)
B10	I/O(F)	D7	I/O(F)	F4	I/O(G)	J3	I/O(G)	M14	GND	R5	V _{CC}
B11	I/O(F)	D8	I/O(F)	F5	I/O(F)	J4	I/O(G)	M15	GND	R6	V _{CC}
B12	I/O(F)	D9	I/O(F)	F6	GND	J5	I/O(G)	M16	GND	R11	GND
B13	CLK(5) /PLLIN(3)	D10	I/O(F)	F7	V _{CCIO} (F)	J6	V _{CCIO} (G)	M21	V _{CCIO} (D)	R12	GND
B14	I/O(E)	D11	I/O(F)	F8	V _{CC}	J21	V _{CCIO} (D)	M22	V _{CC}	R13	GND
B15	I/O(E)	D12	I/O(F)	F9	V _{CCIO} (F)	J22	I/O(D)	M23	I/O(D)	R14	GND
B16	I/O(E)	D13	TMS	F10	GND	J23	I/O(D)	M24	I/O(D)	R15	GND
B17	I/O(E)	D14	I/O(E)	F11	V _{CC}	J24	I/O(D)	M25	I/O(D)	R16	GND
B18	INREF(E)	D15	I/O(E)	F12	V _{CCIO} (F)	J25	I/O(D)	M26	I/O(D)	R21	V _{CC}
B19	I/O(E)	D16	I/O(F)	F13	GND	J26	I/O(D)	N1	TCK	R22	I/O(C)
B20	I/O(E)	D17	I/O(E)	F14	V _{CCIO} (E)	K1	I/O(G)	N2	I/O(H)	R23	I/O(C)
B21	I/O(E)	D18	I/O(F)	F15	V _{CC}	K2	I/O(G)	N3	I/O(G)	R24	I/O(C)
B22	I/O(E)	D19	CLK(8)	F16	V _{CC}	K3	I/O(G)	N4	I/O(G)	R25	I/O(C)
B23	I/O(E)	D20	I/O(E)	F17	GND	K4	I/O(G)	N5	I/O(G)	R26	I/O(C)

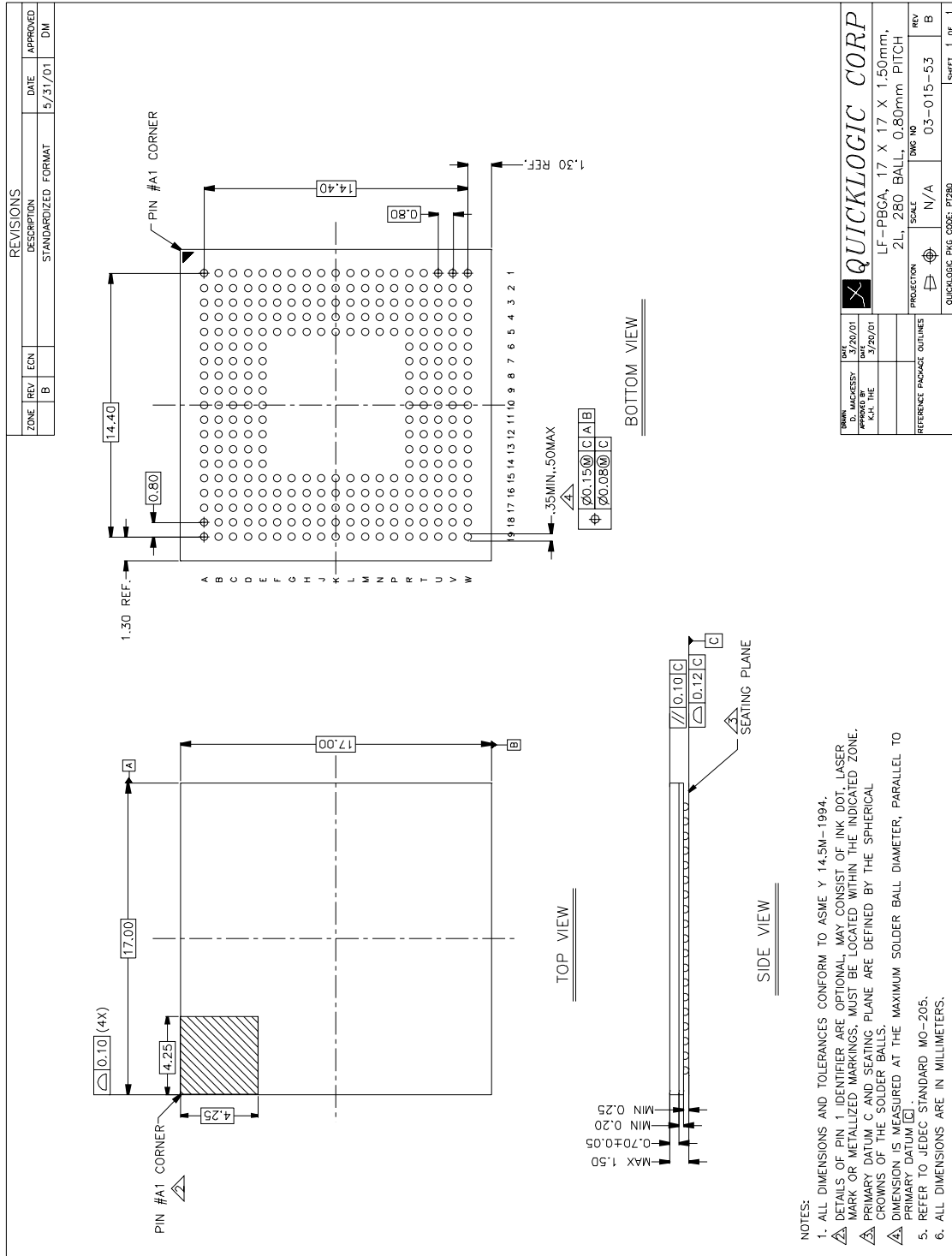
Table 36: 516 PBGA Pinout Table (Continued)

PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function	PBGA	Function
T1	I/O(H)	V22	I/O(C)	AA9	V _{CCIO(A)}	AB20	I/O(B)	AD5	I/O(A)	AE16	I/O(B)
T2	I/O(H)	V23	I/O(C)	AA10	GND	AB21	I/O(B)	AD6	I/O(A)	AE17	I/O(B)
T3	I/O(H)	V24	IOCTRL(C)	AA11	V _{CC}	AB22	GNDPLL(2)	AD7	I/O(A)	AE18	I/O(B)
T4	I/O(H)	V25	I/O(C)	AA12	V _{CCIO(A)}	AB23	I/O(B)	AD8	IOCTRL(A)	AE19	I/O(B)
T5	I/O(H)	V26	I/O(C)	AA13	GND	AB24	I/O(C)	AD9	I/O(A)	AE20	I/O(B)
T6	V _{CC}	W1	INREF(H)	AA14	V _{CCIO(B)}	AB25	I/O(C)	AD10	I/O(A)	AE21	I/O(B)
T11	GND	W2	I/O(H)	AA15	V _{CC}	AB26	I/O(C)	AD11	I/O(A)	AE22	I/O(B)
T12	GND	W3	I/O(H)	AA16	V _{CC}	AC1	I/O(A)	AD12	TDI	AE23	I/O(B)
T13	GND	W4	I/O(H)	AA17	GND	AC2	I/O(A)	AD13	CLK(4) DEDCLK/PL LIN(0)	AE24	I/O(B)
T14	GND	W5	V _{CC}	AA18	V _{CCIO(B)}	AC3	I/O(A)	AD14	I/O(A)	AE25	PLL _{RST} (2)
T15	GND	W6	V _{CC}	AA19	V _{CC}	AC4	I/O(A)	AD15	I/O(B)	AE26	I/O(B)
T16	GND	W21	V _{CC}	AA20	V _{CCIO(B)}	AC5	I/O(A)	AD16	I/O(B)	AF1	I/O(A)
T21	V _{CC}	W22	I/O(C)	AA21	GND	AC6	I/O(A)	AD17	I/O(B)	AF2	I/O(A)
T22	V _{CC}	W23	I/O(C)	AA22	V _{CC} PLL(2)	AC7	I/O(A)	AD18	INREF(B)	AF3	I/O(A)
T23	I/O(C)	W24	I/O(C)	AA23	I/O(C)	AC8	I/O(A)	AD19	I/O(B)	AF4	I/O(A)
T24	I/O(C)	W25	INREF(C)	AA24	I/O(C)	AC9	I/O(A)	AD20	I/O(B)	AF5	I/O(A)
T25	I/O(C)	W26	I/O(C)	AA25	I/O(C)	AC10	I/O(A)	AD21	I/O(B)	AF6	IOCTRL(A)
T26	I/O(C)	Y1	I/O(H)	AA26	I/O(C)	AC11	I/O(A)	AD22	I/O(B)	AF7	I/O(A)
U1	I/O(H)	Y2	I/O(H)	AB1	I/O(H)	AC12	I/O(A)	AD23	I/O(B)	AF8	I/O(A)
U2	I/O(H)	Y3	I/O(H)	AB2	I/O(H)	AC13	I/O(A)	AD24	GND	AF9	I/O(A)
U3	I/O(H)	Y4	I/O(H)	AB3	I/O(A)	AC14	CLK(1)	AD25	I/O(B)	AF10	I/O(A)
U4	I/O(H)	Y5	I/O(H)	AB4	GNDPLL(3)	AC15	I/O(B)	AD26	I/O(B)	AF11	I/O(A)
U5	I/O(H)	Y6	V _{CCIO(H)}	AB5	V _{CC} PLL(3)	AC16	I/O(B)	AE1	GND	AF12	CLK(2) /PLLIN(2)
U6	GND	Y21	V _{CCIO(C)}	AB6	I/O(A)	AC17	I/O(B)	AE2	GND	AF13	I/O(B)
U21	GND	Y22	I/O(C)	AB7	I/O(A)	AC18	I/O(B)	AE3	I/O(A)	AF14	I/O(B)
U22	I/O(C)	Y23	I/O(C)	AB8	I/O(A)	AC19	I/O(B)	AE4	I/O(A)	AF15	I/O(B)
U23	I/O(C)	Y24	I/O(C)	AB9	I/O(A)	AC20	I/O(B)	AE5	I/O(A)	AF16	I/O(B)
U24	I/O(C)	Y25	I/O(C)	AB10	I/O(A)	AC21	I/O(B)	AE6	I/O(A)	AF17	I/O(B)
U25	I/O(C)	Y26	IOCTRL(C)	AB11	V _{CC}	AC22	TDO	AE7	INREF(A)	AF18	I/O(B)
U26	I/O(C)	AA1	I/O(H)	AB12	I/O(A)	AC23	PLL _{OUT} (1)	AE8	I/O(A)	AF19	IOCTRL(B)
V1	I/O(H)	AA2	I/O(H)	AB13	I/O(A)	AC24	I/O(B)	AE9	I/O(A)	AF20	IOCTRL(B)
V2	IOCTRL(H)	AA3	I/O(H)	AB14	CLK(3)/ PLLIN(1)	AC25	I/O(B)	AE10	I/O(A)	AF21	I/O(B)
V3	IOCTRL(H)	AA4	I/O(A)	AB15	V _{CC}	AC26	I/O(C)	AE11	I/O(A)	AF22	I/O(B)
V4	I/O(H)	AA5	I/O(A)	AB16	I/O(B)	AD1	I/O(A)	AE12	CLK(0)	AF23	I/O(B)
V5	I/O(H)	AA6	GND	AB17	I/O(B)	AD2	PLL _{OUT} (2)	AE13	I/O(B)	AF24	I/O(B)
V6	V _{CCIO(H)}	AA7	V _{CCIO(A)}	AB18	I/O(B)	AD3	PLL _{RST} (3)	AE14	I/O(B)	AF25	I/O(B)
V21	V _{CCIO(C)}	AA8	V _{CC}	AB19	V _{CC}	AD4	I/O(A)	AE15	I/O(B)	AF26	I/O(B)

208 PQFP Packaging Drawing

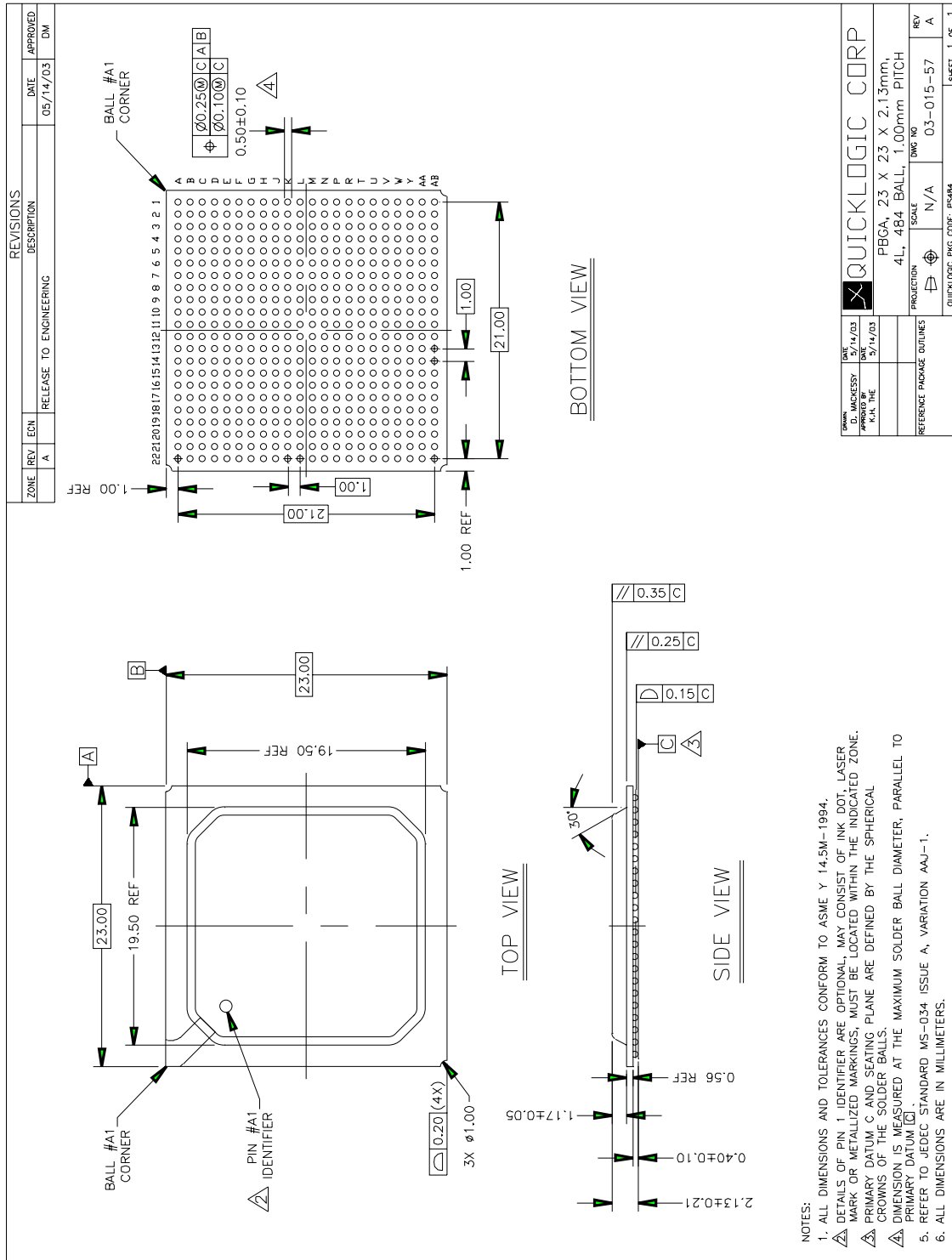


280 LFBGA Packaging Drawing



- NOTES:
- ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y 14.5M-1994.
 - DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, MAY CONSIST OF INK DOT, LASER MARK OR METALLIZED MARKINGS, MUST BE LOCATED WITHIN THE INDICATED ZONE.
 - PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
 - DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
 - REFER TO JEDEC STANDARD MO-205.
 - ALL DIMENSIONS ARE IN MILLIMETERS.

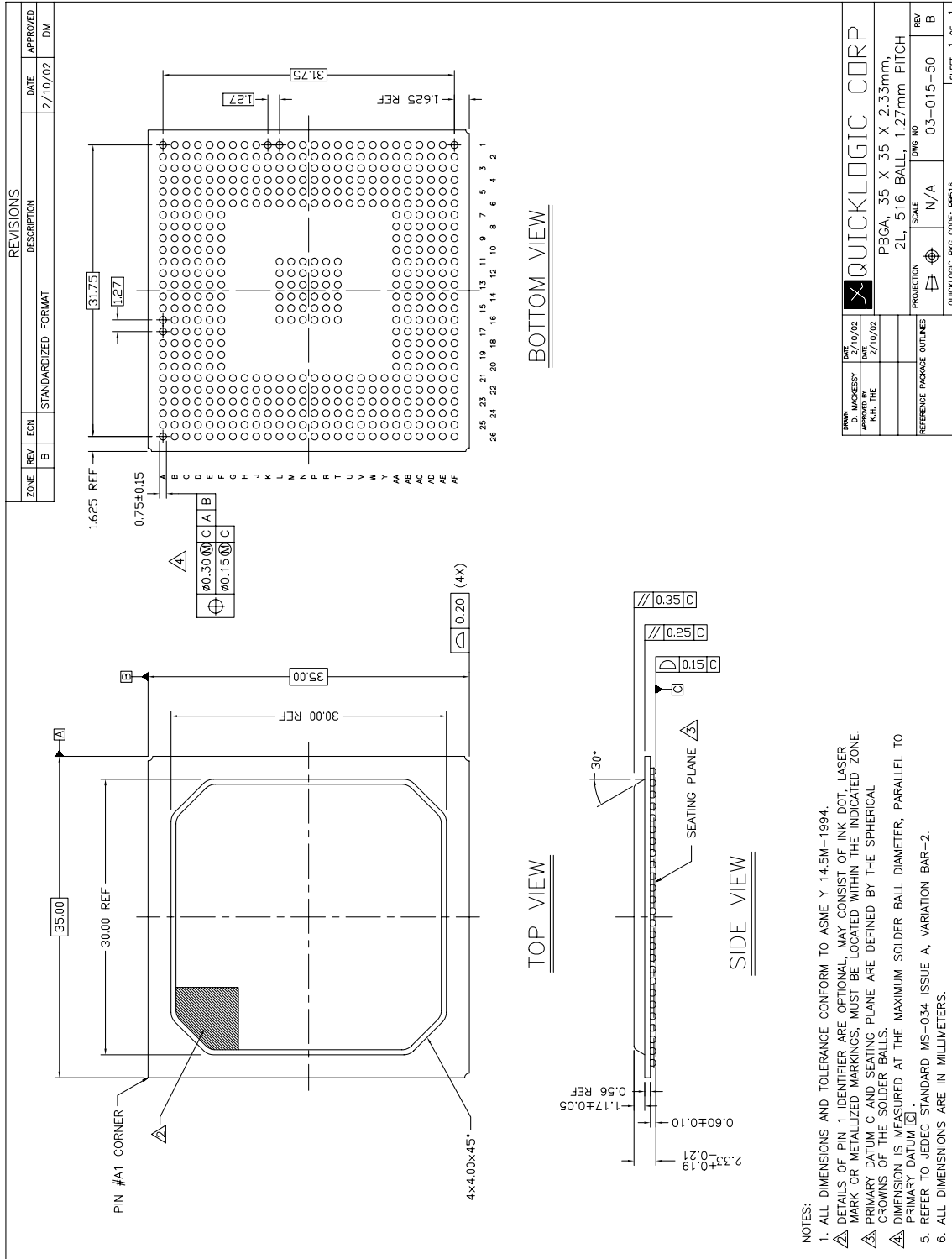
484 PBGA Packaging Drawing



NOTES:

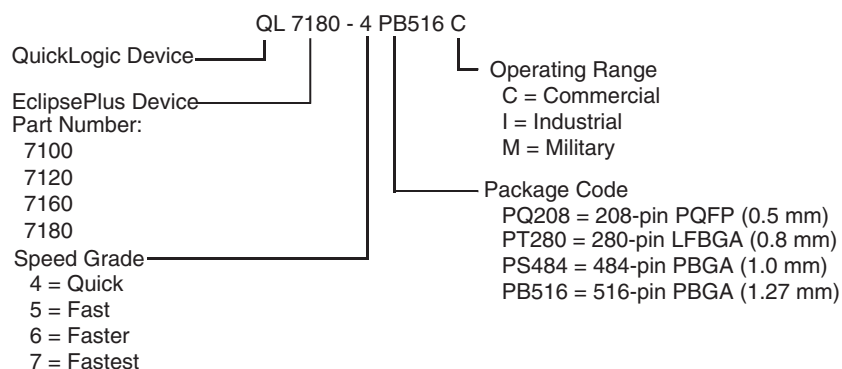
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y 14.5M-1994.
2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL. MAY CONSIST OF INK DOT, LASER MARK OR METALLIZED MARKINGS. MUST BE LOCATED WITHIN THE INDICATED ZONE.
3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
5. REFER TO JEDEC STANDARD MS-034 ISSUE A, VARIATION AAJ-1.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

516 PBGA Packaging Drawing



DESIGN BY MACKESSY	DATE 2/10/02	QUICKLOGIC CORP	PBGA, 35 X 35 X 2.33mm, 2L, 516 BALL, 1.27mm PITCH
APPROVED BY K.H. THE	DATE 2/10/02		
REFERENCE PACKAGE OUTLINES	PROJECTION	SCALE	DWG NO
	1	N/A	03-015-50
QUICKLOGIC PING CODE: P8516			SHEET 1 OF 1

Ordering Information



Packaging Information

The EclipsePlus product family packaging information is presented in **Table 37**.

Table 37: Packaging Options

Device Information	Device							
	QL7100		QL7120		QL7160		QL7180	
	Pin	Pitch	Pin	Pitch	Pin	Pitch	Pin	Pitch
Package Definitions ^a	208 PQFP	0.50 mm	208 PQFP	0.50 mm	280 LFBGA	0.80 mm	280 LFBGA	0.80 mm
	280 LFBGA	0.80 mm	280 LFBGA	0.80 mm	484 PBGA	1.0 mm	484 PBGA	1.0 mm
	484 PBGA	1.0 mm	484 PBGA	1.0 mm	516 PBGA	1.27 mm	516 PBGA	1.27 mm

- a. PQFP = Plastic Quad Flat Pack
 PBGA = Plastic Ball Grid Array
 LFBGA = Low Profile Fine Pitch Ball Grid Array

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Revision History

Revision	Date	Originator and Comments
Rev D	February 2006	Mehul Kochar and Kathleen Murchek

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