Errata Sheet for Arria II GZ Devices

This errata sheet provides updated information about known device issues affecting Arria® II GZ devices.

Introduction

Table 1 lists the specific issues and the affected Arria II GZ devices.

Table 1. Issues for Arria II GZ Devices (Part 1 of 2)

Issue	Affected Devices	Planned Fix
"PLL phasedone Signal Stuck at Low" In some cases, the Arria II GZ phase-locked loop (PLL) blocks exhibit the `phasedone` signal stuck at low during the PLL dynamic phase shift.	All production devices	Quartus II software version 12.0 and later.
"Remote System Upgrade" The remote system upgrade feature fails when loading an invalid configuration image.	All production devices	Software fix
"EDCRC False Error" The error detection CRC (SEU detection) feature may falsely assert the `CRC_ERROR` signal when no SEU event has occurred.	All production devices	—
"PCIe Gen2 Protocol Link Establishment Issue" The PCIe rate switch controller may not be initialized correctly for the PCIe Gen2 protocol, preventing the link from being established.	All production devices	Quartus II 10.1 SP1 and later. Patches are available for the Quartus II software version 10.1.
"Dynamic Reconfiguration Issue Between PCIe Mode and Any Other Transceiver Mode" The transceiver may not be initialized correctly if your application uses dynamic reconfiguration to change the transceiver channel between PCIe mode and any other transceiver mode.	All production devices	No plan to fix silicon. Apply the reset workaround in "Dynamic Reconfiguration Issue Between PCIe Mode and Any Other Transceiver Mode"
"I/O Jitter" Affected Arria II GZ production devices may exhibit higher than expected jitter on general purpose I/O pins.	EP2AGZ300 and EP2AGZ350 devices	Silicon Revision
"Transmitter PLL Lock (pll_locked) Status Signal" The transmitter PLL lock status signal (`pll_locked`) does not de-assert when the `pll_powerdown` signal is asserted in configurations that use the reference clock pre-divider of 2, 4, or 8.	All production devices	No plan to fix silicon. For a soft-fix solution, refer to "Transmitter PLL Lock (pll_locked) Status Signal".

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Table 1. Issues for Arria II GZ Devices (Part 2 of 2)

Issue	Affected Devices	Planned Fix
"M144K RAM Block Lock-Up" M144K RAM blocks may lock up if there is a glitch in the clock source.	EP2AGZ300 and EP2AGZ350 devices	No plan to fix silicon. Apply the workaround in "M144K RAM Block Lock-Up".
"x8 and xN Clock Line Timing Issue for Transceivers" xN clock line performance limits data rates depending on the clock source configuration.	All production devices	No plan to fix silicon.

PLL phasedone Signal Stuck at Low

In some cases, the Arria II GZ PLL blocks exhibit the `phasedone` signal stuck at low during the PLL dynamic phase shift. When the PLL `phasedone` signal is stuck at low, the intended phase shift does not happen. You can recover from the PLL `phasedone` signal being stuck at low by resetting the PLL or by restarting the phase shift operation by asserting the `phasestep` signal.

Solution

To resolve the PLL `phasedone` signal stuck at low issue, the Altera® PLL megafunction is enhanced to automatically restart the phase shift operation internally in the Altera PLL megafunction whenever the PLL `phasedone` signal is stuck at low. Restarting the phase shift operation compensates for the missing phase shift operation and also recovers the `phasedone` signal.

This Altera PLL megafunction solution will be implemented in the Quartus II software version 12.0 and later. Altera recommends upgrading to the latest Quartus II software, regenerating the PLL megafunction, and recompiling your design.

Additionally, software patches are available for the Quartus II software versions 9.1 SP2 and 10.1 SP1 to upgrade the PLL megafunction with the solution. To download and install the Quartus II software patch, refer to the PLL Phasedone Stuck at Low Solution.

If you need additional support, file a service request using mySupport.

Remote System Upgrade

The remote system upgrade feature does not operate correctly when you initiate a reconfiguration cycle that goes from a factory configuration image to an invalid application configuration image. In this scenario, the Arria II GZ device fails to revert back to the factory configuration image after a configuration error is detected while loading the invalid application configuration image. The failure is indicated by a continuous toggling of the `nSTATUS` pin.

In correct operation, the Arria II GZ device reverts back to the factory configuration image after a configuration error is detected with the invalid configuration image.

☞ An invalid application configuration image is classified as one of the following:

- A partially programmed application image

- A blank application image
- An application image assigned with a wrong start address

The remote system upgrade feature works correctly with all other reconfiguration trigger conditions.

This issue is addressed by enabling the Reconfig POF Checking feature in the updated ALTREMOTE_UPDATE megafunction and is available in the Quartus II software version 9.1 and later.

For more information about how to enable the Reconfig POF Checking feature, refer to *AN 603: Active Serial Remote System Upgrade Reference Design*.

EDCRC False Error

The error detection cyclic redundancy check (CRC) (single event upset [SEU] detection) feature may falsely assert the `CRC_ERROR` signal when no SEU event has occurred. This happens because the configuration RAM is incorrectly read for the EDCRC checks. In this scenario, the configuration RAM data and the functionality of the device are not affected.

- If EDCRC is not critical to your system, turn it off.
- If EDCRC is required, insert a soft IP in your design.

For more support and to request the soft IP, file a service request using mySupport.

PCIe Gen2 Protocol Link Establishment Issue

The PCI Express® (PCIe®) rate switch controller may not be initialized correctly for the PCIe Gen2 protocol, preventing the link from being established. When the rate switch controller is not initialized correctly, the transmitted TS1 training sequence is corrupted. This issue occurs intermittently and in some cases, power cycling the device may re-establish the link. This issue affects PCIe Gen2 x1 and x4 configurations with and without the hard IP block. The PCIe Gen1 only configurations are not affected.

Solution

The issue is fixed in the Quartus® II software versions 10.1 SP1 and later. Altera recommends upgrading to the latest Quartus II software, regenerating the IP, and recompiling your design. For complete details of the solution, refer to the PCIe Gen2 Protocol Link Solution.

Additionally, software patches are available for the Quartus II software version 10.1.

To download and install the patch, refer to the PCIe Gen2 Protocol Link Solution.

Dynamic Reconfiguration Issue Between PCIe Mode and Any Other Transceiver Mode

If your application uses dynamic reconfiguration to change the transceiver channel between PCIe mode and any other transceiver mode, the transceiver may not be initialized correctly, resulting in receiver bit errors.

This problem only affects dynamic reconfiguration between PCIe mode and any other transceiver mode. Dynamic reconfiguration between any transceiver modes other than PCIe mode is not affected.

Workaround

If you see bit errors, apply the reset sequence described in the Reset Sequence Solution.

If you need additional support, file a service request at Altera's mysupport.

I/O Jitter

Affected Arria II GZ production EP2AGZ300 and EP2AGZ350 devices may exhibit up to ± 50 ps higher than expected jitter on general purpose I/O pins. Transceiver I/O pins and I/O pins in LVDS mode (including dynamic phase alignment [DPA] and soft clock data recovery [CDR]) are not affected. The actual amount of additional jitter depends on the device switching activity.

The EP2AGZ225 production ordering codes are not affected.

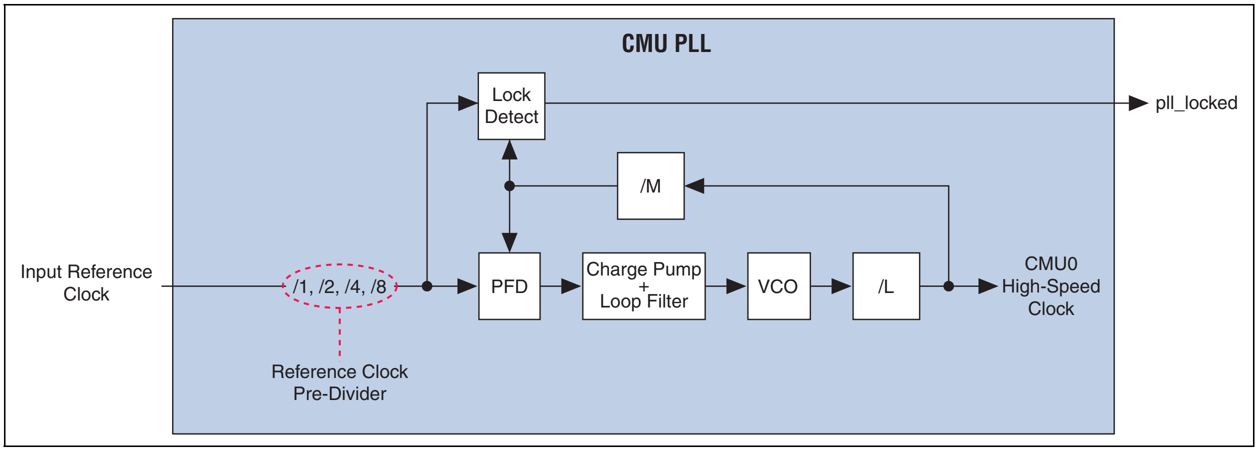
Altera is fixing this issue in the next revision of production devices, which will meet all current jitter specifications.

For further support, file a service request using mysupport.altera.com.

Transmitter PLL Lock (pll_locked) Status Signal

The transmitter phase-locked loop (PLL) lock status signal (`pll_locked`) does not de-assert when the `pll_powerdown` signal is asserted in configurations that use the reference clock pre-divider of 2, 4, or 8. Figure 1 shows the reference clock pre-divider inside transmitter PLLs. This issue impacts the `pll_locked` status signal in the clock multiplier unit (CMU) PLL.

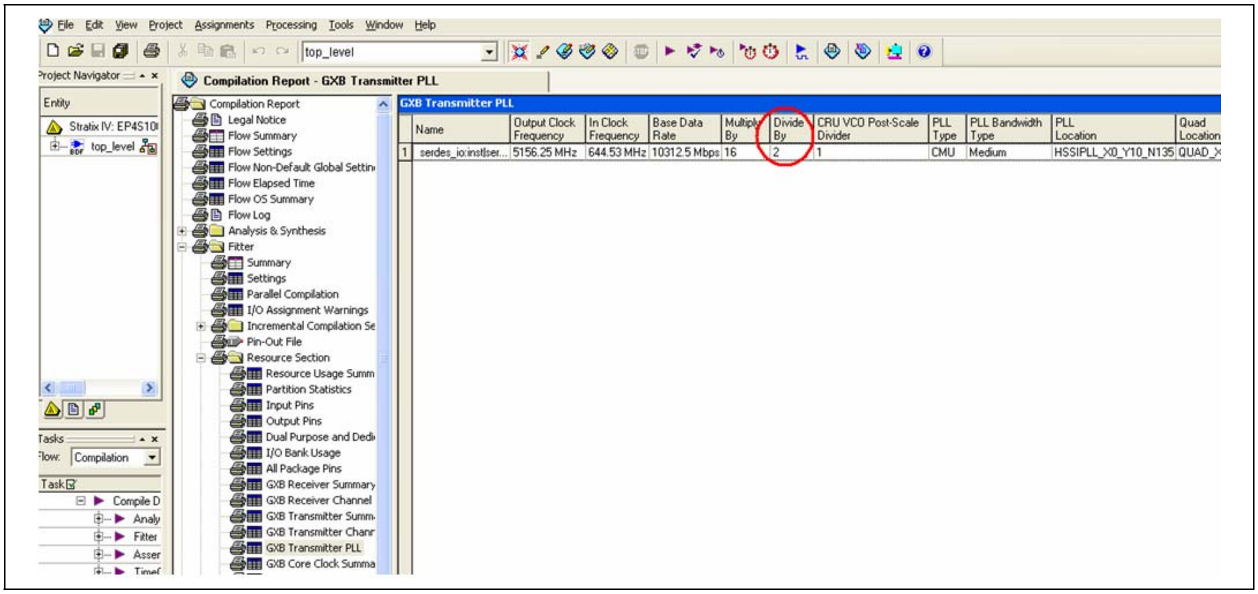
Figure 1. Reference Clock Pre-Dividers in Transmitter PLLs



Designs that implement the recommended transceiver reset sequence described in the *Reset Control and Power Down in Arria II Devices* chapter in volume 2 of the *Arria II Device Handbook* could potentially see a link failure after coming out of reset.

You can determine if the Transmitter PLL in your design uses a reference clock pre-divider of 2, 4, or 8 by referring to the Quartus II software Compilation Report. Figure 2 shows an example of the “GXB Transmitter PLL” report, which you find in the “Resources Section” under “Fitter” in the Compilation Report. If the value in the “Divide By” column reads 2, 4, or 8, your design is impacted by the `pll_locked` status signal issue.

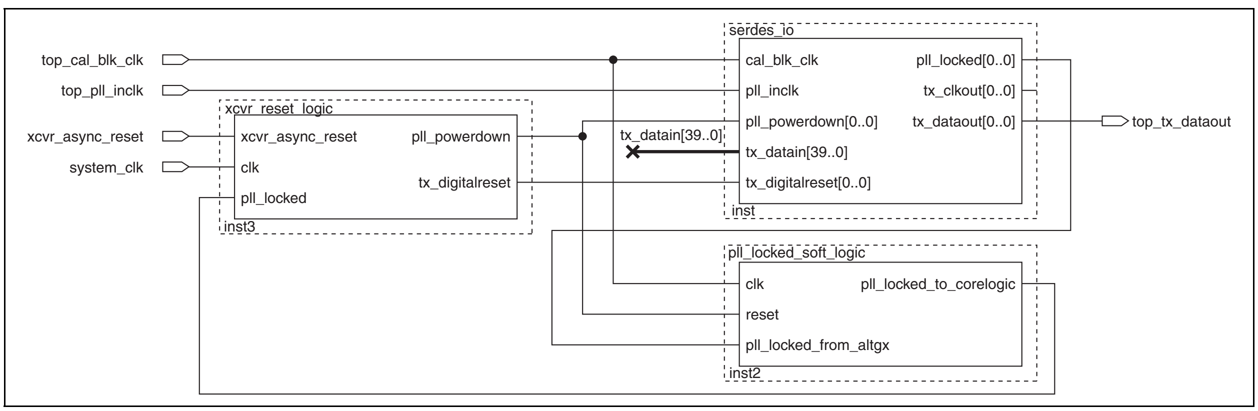
Figure 2. Determining Reference Clock Pre-Divider Value in the Compilation Report



Workaround

If the `pll_locked` issue impacts your design, instantiate and connect the `pll_locked_soft_logic` module, as shown in Figure 3. You must use the `pll_locked_to_corelogic` output from this module in the transceiver reset logic and any user logic that relies on the transmitter PLL lock status signal.

Figure 3. Instantiating and Connecting the pll_locked_soft_logic Module



Click `pll_locked_soft_logic` to obtain the module.

Use the calibration block clock (`cal_blk_clk`) for the `pll_locked_soft_logic` module. The `cal_blk_clk` frequency specification ranges from 10 MHz to 125 MHz. Depending on your `cal_blk_clk` frequency, set the parameter `p_delay_counter` in `pll_locked_soft_logic` so that the delay is equal to 100 µs (worst-case transmitter PLL lock time).

M144K RAM Block Lock-Up

M144K blocks may lock up if there is a glitch in the clock source when `rden` equals 1. In the lock-up state, the RAM block does not respond to read or write operations and requires an FPGA reconfiguration to restore operation. The issue occurs within the M144K RAM in the Read Timer Trigger circuitry. A clock glitch may inadvertently freeze the Read Timer Trigger circuitry, locking the RAM block in its last operation. MLABs and M9K RAM blocks are not affected.

Workarounds

Add clock-enable logic, an internal PLL, or clock-generation logic (for example, a clock divider). You can add clock-enable logic (internal or external) to disable the RAM block operation until the clock is stable. You can also gate the clock internally or externally. If FPGA resources permit, you can use an internal PLL or clock-generation logic to ensure a stable clock source at the RAM block input.

The Read Timer circuitry makes RAM block operation independent of the input clock duty cycle, thus maximizing design performance. If you cannot provide a stable clock, use the **DCD** option in the Quartus II software version 9.1 or later to work around this problem. When the M144K block uses the **DCD** option, it does not exhibit the lock-up behavior, but clock high-time requirements are increased and f_{MAX} performance is degraded.

If you cannot provide a stable clock input without glitches, perform the following steps to enable the **DCD** option in the Quartus II software:

1. On the Assignments menu, click **Settings**.
2. In the **Category** list, select **Fitter Settings**.
3. Click **More Settings**.
4. Under **Existing option settings**, set **M144K Block Read Clock Duty Cycle Dependency** to **On**.
5. Click **OK**.
6. Compile your design.

There is a **.qsf** variable that you can use instead of the previous instructions for making a global assignment.

DCD is on globally by adding the following line to the project's **.qsf** (the default is **Off**):

```
set_global_assignment -name M144K_BLOCK_READ_CLOCK_DUTY_CYCLE_DEPENDENCY
ON
```

Alternatively, you can also apply this setting to individual M144K blocks with the Assignment Editor.

Global and per instance assignments can be mixed. For example, you can set DCD to **On** globally, but set it to **Off** for an instance. You can also only set it to **On** by instance.

x8 and xN Clock Line Timing Issue for Transceivers

The xN clock line timing issue in Arria II GZ production devices affects the maximum data rate supported in the Basic x8 functional mode using the CMU PLL configuration.

The maximum supported data rate in this configuration depends on:

- Transmitter PLL type (CMU PLL)
- Device speed grade
- $V_{CCL\_GXB}/V_{CCT}/V_{CCR}$ power supply level

  The voltage supply levels can be 1.1 V or 1.2 V, depending on the data rate.

- Physical distance between the transmitter PLL and the transceiver channel (refer to the Placement Restrictions column in Table 2)

Table 2 lists the maximum data rate supported in the affected configurations.

Table 2. Maximum Data Rate Specification in ALTGX Functional Modes Impacted by ×N Clock Line Timing Issue

ALTGX Functional Mode	TX PLL Type	Bonding	Supported Data Rates			Placement Restrictions
			Speed Grade	$V_{CCL\_GXB}/V_{CCT}/V_{CCR}$ Supply Level (V)	Max Data Rate (Gbps)	
Basic x8	CMU PLL	Up to x8	C3/I3	1.1	5.0	—
				1.2 ± 0.05	6.375	

The Quartus II software correctly implements the xN line data rate restrictions shown in Table 2 for Arria II GZ production devices. The Quartus II compiler checks for the transmitter PLL type, the distance between the source transmitter PLL and the destination channel in the xN link, and the selected power supply level. If the configured xN line data rate is greater than the maximum data rate supported by the 1.1 V power supply level, but less than or equal to that supported by the 1.2-V power supply level specified in Table 2, the Quartus II Compiler flags the following compilation error:

"Error: Transceiver channels clocked by clock divider atom top_alt4gxb:top_alt4gxb_component|central_clk_div0" are configured at a data rate that is higher than that supported in Arria II GZ devices. The data rate limitation is due to a xN clock line issue.

To remedy this, set the **VCCT_L/R**, **VCCL_GXBL/R**, and **VCCR_L/R** voltage settings from 1.1 V to **1.2 V** and recompile your project.

Document Revision History

Table 3 lists the revision history for this errata sheet.

Table 3. Document Revision History

Date	Version	Changes
June 2012	1.4	Added the "PLL phasedone Signal Stuck at Low" section.
September 2011	1.3	■ Added the "Remote System Upgrade" section. ■ Minor test edits.
June 2011	1.2	Added the "EDCRC False Errors" section.
March 2011	1.1	Added "PCI Express (PCIe) Gen2 Protocol Link Establishment Issue" section.
December 2010	1.0	Initial release.